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REVIEW ARTICLE

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POWER-AWARE DESIGN-FOR-TESTABILITY IN SEMICONDUCTOR DEVICES: A REVIEW OF ENERGY-EFFICIENT TESTING STRATEGIES

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***Abstract*—**The development of new testing techniques to prolong the life of semiconductors is seen as an important issue in integrated circuit (IC) design as new fabricated devices in the manufacture of semiconductors keep increasing in complexity and performance. Any excessive power use demonstrated in the testing may lead to yield loss, failure due to IR drop, thermal reliability issues, and overdesign. This review gives an outset exploration of the field of power-aware Design-for-Testability (DfT) methods and practices that are used to reduce the power consumption of designs under test (both dynamic as well as static power) as the test coverage of the design remains high. Important areas are low-power scan architectures, power savings via shift, scan chain reordering, compressed test patterns and power-limited automatic test pattern generation (ATPG). Emerging developments that are also discussed by the paper include 3D IC-aware DfT, AI-based test generation, and security-integrated low-power testing. The discussed strategies are assessed by their contribution to green chip production, thermal control and cost-effectiveness in modern System-on-Chip (SoC) designs. Additionally, another challenging issue under critical review is the power-thermal correlation, the increasing volume of test data, and test access overheads. The research opportunities ahead incorporate the concept of machine learning, real-time monitoring of power, context-sensitive test scheduling so that scalable, secure, and energy-aware semiconductor testing systems can be supported.

***Keywords*—**Power-Aware Testing, Design-for-Testability (DfT), Automatic Test Pattern Generation (ATPG), Energy-Efficient IC Testing, Semiconductor Devices**.**

I. INTRODUCTION

The growth of semiconductor testing has closely followed that of the field of integrated circuits (ICs) as a whole [1], particularly as more complex circuits emerged and their performance requirements also increased. The relentless pursuit of Moore's Law by the semiconductor industry has resulted in significantly increasing transistor densities, and in turn, very high design and testing requirements.

Design and verification have also demonstrated significant levels of integration with the concepts behind Design for Testability (DFT), which offers a solution to such complexities [2]. DFT increases the observability and controllability of internal circuit nodes, enabling end-to-end fault detection, diagnosis, and improved test coverage.

At the same time, increasing power efficiency is a significant limitation in ICs, where energy efficiency is a major target in applications such as mobile computing, IoT, AI, and high-performance computing [3]. Large power consumption generally impacts the reliability of systems, the level of heat dissipation, and the battery's durability in portable machines. Therefore, methodologies of estimating and reducing power have become the focus of semiconductor design as well as testing strategies optimization efforts.

In this regard, Power-Aware Test is proposed as a new and unique field of study [4]. It entails not only reducing the consumption of power during a test, but also executing proactive power profiling as a way of providing intelligent perspective on the effective test planning and implementation [5]. Such tactics play a vital role in reducing both dynamic and static power consumption during test operations, while also improving yield without compromising test quality.

Scan chain optimization is a major target of interest in Power-Aware Testing. Scan chains are used to enhance the testability of ICs; however, it has been noted that a significant portion of the power generated in ICs is due to scan chains, resulting from flip-flop toggling during testing by applying test patterns [6]. Research has focused on minimizing delay and power overheads through methods such as optimized chaining and gating.

In addition to technical advancements, the environmental implications of the semiconductor industry have come to the fore [7]. With semiconductors the foundation of the modern digital infrastructure, driving everything in the world as know it, including smartphones as well as renewable energy generation systems, demand is increasing to make production and testing sustainable [8]. This involves reducing carbon footprints by applying energy-efficient technology, recycling, and utilizing and maintaining effective policy systems. To facilitate this key development in semiconductor innovation, interdisciplinary communication among researchers, industry leaders, and policymakers is necessary to direct the course of semiconductor development toward the most sustainable variants [9]. Power-aware DFT and test strategies are necessary not only for optimizing technical performance and reliability, but also for the concept of environmentally sound innovation in the semiconductor industry.

A. Structure of the paper

This paper is organized as follows: Section II gives a summary of power-related issues in IC testing. Section III examines energy-efficient Design-for-Testability (DFT) efforts together with exploitation strategies. Section IV highlights recent developments, such as AI-based testing. Sections V and VI present future research directions that could be pursued to maximize power-aware testing of semiconductor devices.

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II. Understanding The Core Concepts Of Design-For-Testability (DFT)

As semiconductor technologies scale, the issue of controlling unwanted power dissipation during the testing of integrated circuits (ICs) becomes increasingly acute. In most instances the dissipated power in test mode is higher than during the normal functional operation and this may lead to high thermal stress, lower manufacturing yield and even reliability issues including degradation or premature failure of the device itself [10]. To overcome them, power-based Design-for-Testability (DFT) solutions have developed, which incorporate energy-efficient components into the test structure. These methods are multi-voltage testing, clock gating, scan chain segmentation or partitioning, and dynamic power control or power management, all of them designed to eliminate problems with excessive switching activity, scan chain loading, and peaks, introduced by test compression. In addition, the sophisticated DFT techniques currently include power-sensitive metrics and design rules that ease the production of test patterns and scheduling plans, promoting minimal power consumption.

A. Importance of Low-Power Testing in Modern ICs

Integrated circuit (IC) design is still evolving towards achieving miniaturization, increased integration levels, reliability, and improved performance. High-performance, high-end chips have gained a fundamental status in a variety of industries, including communications, computing, aerospace, and consumer electronics. Advancing Very-Large-Scale Integration (VLSI), which is one of the factors that have propelled this advancement, has led to prevalent use of computer technology in the design of ICs. These developments have significantly enhanced the growth of the semiconductor industry, which, in addition to technological advancements, has also contributed to societal development and is considered a key factor in human civilization. As complexity escalates in ICs, testing low power use can no longer be ignored as it is the only way to guarantee energy efficiency, yield and avert heating or damage in testing the contemporary semiconductor technology devices.

Integrated circuit design is undergoing continuous transformation towards miniaturization, high integration, high reliability and high performance. Many high-end and high-performance chips have been essential in the communications, computer, aerospace, and household appliance industries. Due to today's rapid developments in Very-Large-Scale Integration (VLSI), computer technology has been widely applied in the field of IC design, significantly promoting the growth of the integrated circuit industry and making substantial contributions to the advancement of society and human civilization [11]. Several low-power voltage design techniques are given below:

- **Multi-Voltage-Source Technology:** In complex chips, different modules operate at varying voltage levels. High-performance units, such as the CPU, may require higher voltage, while others operate efficiently at lower levels, which helps reduce overall power consumption.
- **Circuit Automatic Control Unit Technology:** This digital integrated circuit's autonomous control unit (or power management control unit) may monitor and control the operation of certain on-chip components.
- **Clock Gating Technology:** Clock locking technology may still be the most effective low-power method used today. When this clock-gating technology isn't used, the same value is put into the next registers at the beginning of every clock cycle, which wastes power.

B. Sources of Excessive Power Dissipation During IC Testing

Complementary metal-oxide semiconductor (CMOS) technology has allowed for exponential rise in transistor densities, allowing for greater functionality to be integrated on a silicon wafer, thanks to the continuous scaling of feature size [12]. Power densities have continued to rise despite the linear decline in supply voltage that has followed the expansion in transistor density. One issue with high power densities is providing enough power for the circuit to operate, and another is the heat flow that results from dissipation. Supply integrity issues may arise due to power delivery difficulties. The practical functioning of electronics is not the only domain in which power concerns manifest. During testing, the usual power management systems are typically turned off, resulting in higher power usage [13]. Key sources of power inefficiency include:

- **Switching activity:** Automatic test pattern generation (ATPG) is notoriously complicated, thus most tests are conducted structurally.
- **Compared to functional:** modes like scan, design-for-testability (DFT) circuitry is used and puts a lot of stress on the circuit-under-test (CUT).
- **Power availability and quality:** It increases the manufacturing yield loss and tester power supply (TPS)
- **Bus contention problem:** Illegal circuit operation, such as short-circuit power dissipation from VDD to ground, can be caused by non-functional vectors during structural testing.
- **Simultaneous Activation of Logic Paths:** During testing, multiple switching events may occur concurrently across various logic paths, leading to excessive dynamic power consumption and potential thermal issues.
- **Clock Gating Inactivity:** Clock gating, typically used to reduce power during normal operation, is often disabled during testing, resulting in unnecessary power usage in inactive regions of the circuit.
- **Test Compression Overheads:** Test compression techniques, while reducing test data volume and time, can increase switching activity and power consumption due to high toggling rates during decompression.
- **Inadequate Power-Aware DFT Design:** Design-for-Testability strategies that neglect power constraints can lead to inefficient test patterns and elevated power usage, compromising chip reliability during test.

C. Metrics for Evaluating Power-Efficient Testing (Peak power, average power, thermal profile)

Electrical power is a valuable resource, and all types of computers, from cell phones to data centres, need to use it efficiently. Achieving power consumption that is directly proportional to the computational effort expended, or power proportionality, has been a primary goal of these optimizations [14]. Optimizing power consumption across the entire platform requires a smart, dynamic power management (DPM) system, as energy-efficient components become increasingly important. The paper examines the power consumption of various GPU architectures and finds that algorithms can be grouped into two categories based on their power consumption: computationally intensive and data transfer-heavy. In addition, the EC analyzes data transmission between the CPU and GPU, specifically the CPU's utilization of dynamic voltage and frequency scaling (DVFS), which provides a methodology for identifying the ideal CPU frequency in particular [15]. The optimized DVFS settings improve the EC and CP of GPU and CPU systems alike. It should be noted that in this instance, the external measuring

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system implemented accommodates the application's interests. Presented below are the essential points concerning power supply and thermal profile:

- There is a tight relationship between high-density printed circuit board (PCB) power delivery and heat control.
- Poor power delivery can lead to voltage drops and power noise [16], resulting in increased heat generation. Inadequate thermal management can degrade power delivery performance by affecting component reliability and efficiency.
- It is necessary to address both aspects simultaneously in a holistic way to maximize the performance of the system as a whole.
- Effective design involves incorporation of power and thermal considerations early during the process of PCB development.
- Prediction and mitigation of possible power and thermal problems during the design phase ought to be carried out using simulation tools.

One of the most crucial aspects of high-density printed circuit board designs is efficient power distribution and thermal management; these two factors are intricately linked and can significantly impact the system's performance and reliability. Both aspects should be integrated as early as possible with the help of simulation tools to make the operation of hardware more stable and optimized.

III. Energy-Efficient Scan Design And Test Pattern Optimization

Power management during testing is now essential for ensuring performance and reliability of increasingly sophisticated and smaller semiconductor devices. An essential part of power-aware Design-for-Testability (DfT) is scan-based energy efficiency, which encompasses low-power scan topologies, test data compression, and thermal-aware test creation. 3D integrated circuits have made great strides in reducing switching activity, heat accumulation, and power overhead with innovations such as scan chain gating, selective compression techniques, and temperature-aware scheduling. Together, these approaches enable optimized test performance with minimal energy usage, aligning with the growing demand for environmentally friendly and economically viable IC testing in modern electronic systems.

A. Low-Power Scan Architectures (E.G., Scan Chain Reordering, Gating Techniques)

In today's Design-for-Testability (DFT) paradigm, low-power scan architectures are necessary to eliminate undesirable power consumption through scan testing. Scan-based testing is widely employed to ensure high fault coverage in digital systems, including cryptographic hardware deployed in Wireless Sensor Networks (WSNs) [17]. These networks, used in diverse fields such as healthcare, military, industrial monitoring, and smart infrastructure, demand secure and reliable operation [18]. Cryptographic circuits, being power-sensitive and security-critical, require efficient and low-power testing strategies. Techniques such as scan chain reordering and clock gating are implemented to reduce switching activity and dynamic power consumption during test mode, thereby preserving circuit integrity and prolonging device lifespan

Moreover, power consumption during scan testing becomes a more serious problem as the number of transistors and the complexity of chips is increased. Excessive power consumption reduces circuit reliability and results in yield loss due to IR drop; therefore, minimizing test power consumption is crucial [19]. A novel gating scan structure for shift power reduction considering both the scan chain and the combinational part with the following features:

- Reducing unnecessary shift-mode scan-cell-combinational logic transitions
- Diminutive scan-cell switching activity during shift mode.

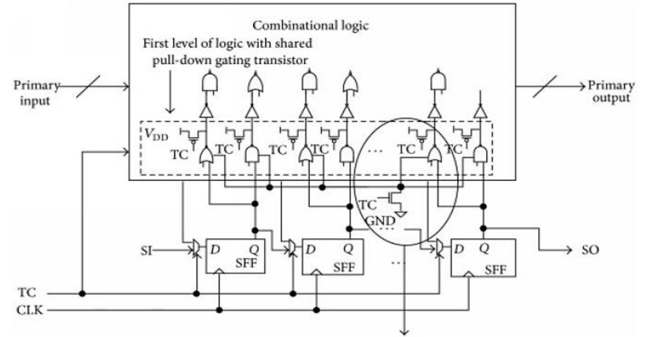

Fig. 1. Low-Power Scan Architecture

A low-power scan-based DFT architecture using clock gating and shared pull-down gating transistors to reduce dynamic power during testing (as shown in Figure 1). Scan flip-flops (SFFs) form a scan chain controlled by a test clock (CLK) and test control signal (TC). The first level of combinational logic shares a gating transistor to limit switching activity. This design minimizes power consumption while maintaining test effectiveness. Modifying the slave latch in the standard master-slave scan cell with state-preserving and gating ability enabled us to achieve the aforementioned qualities within an integrated structure.

B. Test Pattern Compression and Reduction Methods

The continuous scaling of semiconductor technology into the ultra-deep sub-micron (UDSM) regime has significantly increased the integration density and complexity of integrated circuits (ICs). This escalation directly impacts the cost and duration of manufacturing tests [20]. Scan-based testing has emerged as a standard industry practice for validating digital ICs using ATE. However, the resulting increase in test data volume presents challenges in terms of storage, bandwidth, and testing time. To address these issues, efficient test pattern compression and reduction techniques are critical for minimizing test application time, reducing memory requirements on ATE, and lowering overall production costs. One widely adopted reduction method is don't care bit (X-bit) filling, which utilizes unspecified input bits to optimize pattern encoding and significantly reduce the number of required test vectors.

The compressed scan chain (CSC), all test patterns are compressed, for the normal scan chain (NSC), all test patterns are uncompressed. The first group uses compressed shift-in patterns. The second group uses uncompressed patterns. A specialized decoder is required for decoding compressed patterns. Both the original and compressed scan chains are shown in Figure 2, which is a 3-bit decoder construction. The coding results are subject to 23 conditions [21]. As test data, each condition supplies the normal scan cell with decoding results. Using this design as a foundation, split the initial scan chain into numerous scan chains to achieve extremely low power consumption.

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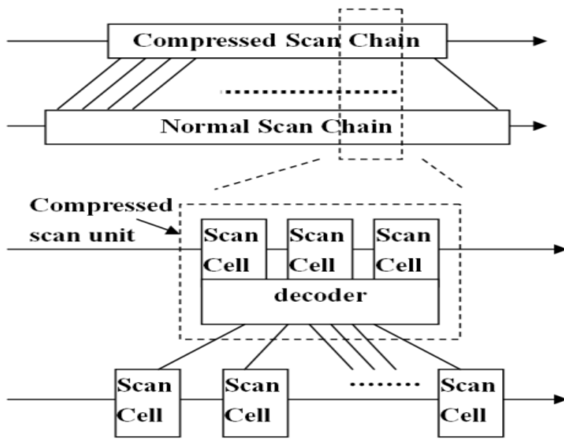

Fig. 2. The Selective Pattern-Compression Architecture, Including Compressed Scan Units.

A larger compression ratio can be achieved using a test set with more undefined bits. To account for both the average power reduction of the remaining test sets and test sets with more unknown bits for test data compression, the LP-SPC technique is suggested. In other words, split the test sets in half according to the number of unknown bits they contain. The user determines the border value that divides the patterns into two categories. Each boundary value provides compression ratio and power reduction for various circuits. To achieve high test data compression, undefined bits in the test data compression (TDC) group, which contains the remaining test sets, are filled in. There is no breach of the peak-power restriction in the resulting patterns.

C. *Thermal-Aware and Frequency-Aware Test Pattern Generation*

The use of 3D integrated circuits (3D ICs) offers hope for integrating heterogeneous systems and scaling processes. Incorporating dynamic thermal profiles into a rectangular 2D bin packing allows for the solution of the test scheduling problem. Using a resource conflict graph, an optimization-based approach was developed for scheduling thermal-safe tests. A 2D thermal resistance model is used to verify if the thermal limitation is satisfied when a test schedule is obtained. A new model for optimizing the scheduling of 2D IC tests based on thermal resistance has been proposed, leveraging the superposition concept. To determine the best solution, you can utilize integer linear programming (ILP). Due to the necessity of examining all potential permutations, the issue size may increase exponentially when thermal limitations are considered. Former research suggested a strategy for scheduling 3D IC tests at the die level. Optimal TAM assignment and test scheduling can only be achieved with thermal-aware co-optimization [22]. These are the three most crucial findings:

- The test time is considered TAM-limited when the quantity of TAM is less than a certain threshold. Presently, including TAM aids in shortening test duration.
- Temperature limits the amount of time the test can last when the number of TAM exceeds the threshold. There is currently no return on investment in terms of reduced test time from including TAM.
- The soft-die mode results in a more efficient reduction of test costs when compared to the hard-die mode. Optimizing the whole 3D IC also involves fine-tuning the Daft architecture of each core.

IV. Advanced DFT Strategies And Emerging Trends

The evolution of semiconductor technologies, particularly 3D ICs, SoCs, and MScs, requires advanced, power-aware Design-for-Testability (DfT) solutions to address the increasing complexity and energy constraints. Recent innovations include adaptive on-chip power monitoring, AI-driven test planning, and the integration of power-efficient architectures in heterogeneous systems. Security-aware and green testing methodologies are also gaining traction, addressing both energy consumption and environmental impact. These strategies enable smarter, sustainable, and secure testing for next-generation devices. By leveraging predictive analytics, ML, and parametric modelling, modern Daft frameworks optimize energy usage without compromising quality, marking a transformative shift in semiconductor test engineering.

A. *Adaptive and On-Chip Test Power Monitoring Techniques*

The development of AI, the IoT, electric vehicles, and similar technologies has significantly accelerated the growth in global integrated circuit (IC) demand, outpacing initial industry forecasts. Within all categories of ICs, system-on-chip (SoC) devices have held a larger market share in recent years, thanks to their higher degree of integration. However, testing them has emerged as a primary challenge, particularly in manufacturing, due to unprecedented design complexity, mixed-signal testing, and higher operating frequencies As shown in Figure 3, each device under test (DUT) undergoing SoC testing and characterization may have four possible outcomes. Among all the outcomes, test escapes are the most harmful.

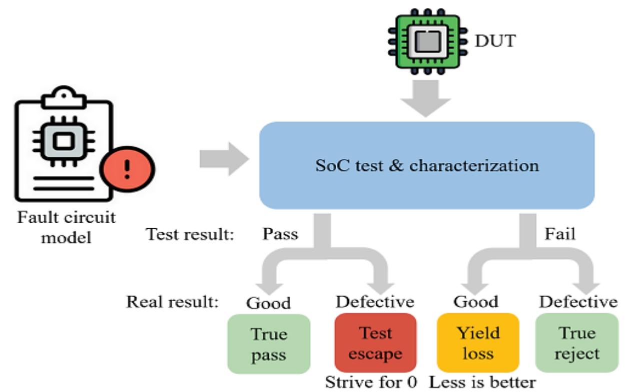

Fig. 3. SoC Test Result Classification.

Product quality is directly proportional to the test coverage; a lower sift rate indicates better coverage [23]. Here are a few ways to enhance the coverage of your tests:

- At-Speed DFT: Due to the difficulty of achieving high coverage requirements with functional test methods before the advent of LSI and VLSI, structural tests like SCAN have become frequently employed.
- Cell Aware Test: The Cell Aware Test checks every standard cell for transistor defects, open circuit situations, and internal particular short circuits.
- IDDQ Test: Conventional complementary metal-oxide-semiconductor (CMOS) chips do not have a direct current (DC) link to the power source and do not conduct electricity when idle.
- LBIST Test: Built-in test vector generation and output vector comparison circuits in logic built-in self-test (LBIST) can make testing more efficient, lessen the load on testers, and lower test costs.

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B. Integration of Power-Aware DFT in 3D ICs and Heterogeneous SoCs

3D ICs, enabled by through-silicon vias (TSVs), represent a significant advancement over traditional 2D ICs, offering notable benefits such as enhanced performance, lower power consumption, and reduced footprint. In TSV-based 3D ICs, individual dies are fabricated using standard 2D CMOS processes and stacked vertically. This vertical integration minimizes interconnect length, reducing signal delay and dynamic power dissipation.

According to the Heterogeneous Integration Roadmap (HIR), 3D ICs and heterogeneous system-on-chip (SoC) architectures are fundamental to advancing next-generation technologies, including IoT, mobile platforms, data centers, and automotive systems [24]. These systems require increasingly complex and efficient designs, prompting the adoption of multiprocessor SoCs (MPSoCs) that incorporate diverse components. The key characteristics of modern MPSoCs include:

- Contemporary applications and System-on-Chip (SoC) designs have become increasingly complicated, greatly expanding the design space for embedded systems.
- This led to the widespread adoption of MSc platforms, which enable the integration of diverse and intricate components. Most of the time, these MPSoCs are diverse and comprise.
- Modules for Memory (such as Cache, SRAM, and FIFO)
- Digital signal processors (DSPs and GPPs)
- Connecting parts (such as Bus, Crossbar, and NoC)
- I/O devices and logic modules that can be reconfigured.

Given the vast design space, energy efficiency and testability must be co-optimized during the design exploration process. Accurate power modelling and estimation tools are essential for evaluating configurations and guiding power-aware design-for-testability (DfT) integration [25]. These tools typically rely on parametric power models to assess both software and hardware power consumption across different abstraction levels.

Furthermore, integrating power-aware DfT strategies into 3D IC and heterogeneous SoC designs introduces unique challenges:

- Thermal issues due to stacked layers during testing, which may affect reliability.
- Increased signal complexity, including inter-die delay and test access difficulty.
- Need for power-constrained test generation to prevent damage during testing of sensitive or tightly packed dies.

To address these challenges, power-aware DfT must be supported by:

- Advanced test scheduling and compression techniques, tailored for 3D architectures.
- Thermal-aware test pattern generation, mitigating heat build-up in densely packed stacks.
- Power-efficient scan chain design across multiple dies and functional blocks.

The integration of power-aware DfT into 3D ICs and heterogeneous SoCs is critical for achieving test efficiency without compromising energy constraints, reliability, or performance [26]. It requires a synergistic approach that combines architectural innovation, accurate power modeling, and advanced test methodologies.

C. Future Directions: AI, Secure, and Green Testing

Future directions include AI-driven test planning for smarter fault detection, security-aware testing to ensure hardware integrity, and green methodologies to minimize energy use and environmental impact. There are some key points given below:

- **AI Integration in Low-Power Design Verification:** A major step forward in the industry, AI integration in low-power semiconductor design verification tackles the growing complexity and demands of contemporary electronic products [27]. Improving predictive maintenance and manufacturing processes with AI leads to higher-quality output and better yields, and it also opens up new market opportunities [28].
- **Security-aware Testing:** The increasing complexity and criticality of semiconductor devices, alongside the evolving landscape of security threats, make the field of semiconductor security verification ripe with opportunities for future research [29].
- **The Rise of Machine Learning in Security Verification:** The semiconductor industry was increasingly turning to ML to enhance security. By training algorithms on vast datasets, ML offered a powerful new way to create more secure and resilient chips for an increasingly complex digital world.
- **Standardization and Collaboration**: Crucial realization was dawning in the semiconductor world: enhancing security was not a solo endeavor, but a team effort.
- **Green Test Methodologies:** Technological innovation and process optimization are necessary for effective mitigation. Important steps include developing next-generation lithography, implementing intelligent control systems, enhancing plasma and chemical vapour deposition methods, and substituting gases with high global warming potential. Reducing Scope 2 emissions has been a particular focus of renewable energy adoption, waste heat recovery deployment, and energy efficiency investment efforts [30]. Similarly, there are practical solutions to reduce resource consumption and environmental damage through material recovery and chemical recycling.

V. Literature Review

This section reviews recent studies on power-aware design-for-testability in semiconductor devices, highlighting advances in scan-based testing, scheduling, fault detection, and thermal-aware methods. Table I summarizes key studies on power-aware testability techniques in semiconductor devices, highlighting their focus areas, methodological approaches, major findings, associated challenges, and proposed future directions for enhancing energy-efficient and scalable testing strategies.

Paria et al. (2025) introduced LITE, an innovative ATPG-aware lightweight scan instrumentation method that uses scan chains' functional flip-flops to make scalable, low-cost, and numerous internal nodes observable and controlled. To achieve good test quality at a low hardware cost, scan-based Design-for-Testability (DFT) approaches are widely used in current digital integrated circuits. The ability of scan to make internal design nodes configurable and viewable in a systematic and scalable way is making it an increasingly significant role in 3D heterogeneous integration and chiplet-based systems. One drawback of scan-based DFT is that it isn't very good at testing

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complicated circuits at deep logic levels, especially their internal nodes. Test Point Insertion (TPI) is the primary solution for addressing this issue, particularly in nodes that lack good controllability or observability [31].

Xun et al. (2024) propose a Daft based on a parallel-reference write circuit that can detect all single-cell RRAM array faults, including both strong and weak faults. The scheme replaces the regular write driver and enables the monitoring and comparison of the write current against multiple references during a single write operation. However, due to the immature manufacturing process, RRAMs are prone to exhibiting new failure mechanisms and faults, which should be efficiently detected for high-volume production. Some of these faults are difficult to detect and require a specific Design-for-Testability (DfT) circuit design. The results of the simulations performed do not only show that the DfT can detect single-cell conventional faults (due to interconnects and contacts) as well as unique RRAM faults (based on silicon data) that have been demonstrated to exist, but also that the DfT is robust to process variations [32].

Liang et al. (2023) provide test applications with power and temperature forecasts. Employ decay surface models for temperature predictions and multiple ML models for power predictions to save runtime, respectively. Avoid using internal logic values from gate-level simulation and instead build features from flip-flop values, which helps conserve storage. A power prediction MAPE of less than 8% was achieved by us. Their MAE for temperature prediction is under 1.2 °C. With a storage reduction of 118 times and a runtime speedup of 75 times, the transient thermal analysis of extended ATPG patterns performs admirably. Optimal test time and thermal safety can be achieved with forecasts because they scale with test speed [33].

Habiby, Huhn and Drechsler (2022) present a completely automated test scheduling framework for IJTAG test networks, which incorporates two innovative power-aware test scheduling methods—one based on integer linear programming and the other on pseudo-Boolean optimization—to handle test networks with different power domains. With a manageable run-time requirement, the first optimisation approach that has been suggested can find a local optimal test schedule, making it suitable for networks with over a thousand sensors. In addition, no other method currently available comes close to matching the performance of the second optimisation methodology, which finds a globally optimal test scheduler and is hence ideal for medium-sized networks [34].

Lee et al. (2021) address this issue by proposing a novel approach to rearrange scan clusters that considers scan correlation. Using a new scan correlation-aware clustering algorithm, the proposed approach places scan cells with strong correlation close to each other. In order to ensure the quality of cryptographic circuits, which are used to secure wireless sensor network applications, testing is done during manufacture. Consequently, to increase testability, a scan design is commonly employed for manufacturing-stage circuit testing. Scan testing does use electricity, but as chip complexity and transistor count rise, the power consumption of the test becomes increasingly noticeable. Achieving a substantial reduction in power consumption without requiring excessive computational time remains a challenging task. The authors of this work present a novel method for sorting scan clusters that considers scan correlation [35].

Li et al. (2021) presented an innovative, evolutionary learning-based low-power controller that considers testability. By utilising adaptive control for scan chains based on their utilisation, the XORNet produced by the suggested genetic algorithm (GA) significantly enhances XORNet encoding capacity, reduces the frequency of failure instances with ATPG, and minimises test data storage. Unfortunately, without proper design direction, current systems that use an equal construction of the XORNet for scan chain management run the risk of producing poor results. Using the same control bits, GA-guided XORNet design can improve fault coverage by up to 2.11%, according to experimental results [36].

TABLE I. COMPARATIVE ANALYSIS OF RECENT RESEARCH ON LOW-POWER TESTABILITY TECHNIQUES AND OPTIMIZATION STRATEGIES IN SEMICONDUCTOR DEVICES

Reference	Study On	Approach	Key Findings	Challenges	Future Direction
Paria et al. (2025)	Lightweight scan-based DfT for complex digital circuits	LITE – ATPG-aware scan instrumentation using functional flip-flops	Enhances observability and controllability in a scalable, low-cost manner	High design cost in traditional TPI methods; limited testability at deeper logic levels	Expand LITE framework for 3D ICs and heterogeneous integration systems
Xun et al. (2024)	DfT for single-cell RRAM fault detection	Parallel-reference write circuit to detect strong/weak faults	Accurately detects hard-to-find RRAM-specific faults and is robust to process variation	Immature RRAM manufacturing leads to diverse fault types	Tailor DfT designs for emerging memory tech and improve scalability for high-volume production
Liang et al. (2023)	Power and thermal prediction for scan-based testing	ML-based prediction using flip-flop value-based features	Achieves <8% MAPE for power, <1.2°C MAE for thermal with large runtime/storage reduction	Dependence on ML model accuracy; limited internal gate-level info	Expand to real-time test optimization and thermal-safe scheduling
Habiby, et.al. (2022)	Smart scheduling of IJTAG test networks with consideration for power	Pseudo-Boolean & ILP-based scheduling optimization	Facilitates effective and scalable test scheduling for networks containing numerous power domains	Managing large-scale networks and balancing local/global optimizations	Develop hybrid scheduling methods and integrate with runtime thermal control

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Lee et al. (2021)	Power reduction in scan testing of cryptographic circuits	Scan correlation-aware scan cluster reordering	Reduces test power by clustering highly correlated scan cells	Complexity increases with chip size and transistor count	Explore AI-driven clustering and an adaptation method to secure SoCs
Li et al. (2021)	Low-power controller for scan-based testing	GA-guided XORNet encoding for scan chain control	Improves fault coverage and reduces power consumption and test data volume	Existing XORNet designs lack adaptability; risk of suboptimal solutions	Enhance adaptive learning for real-time control and explore multi-objective optimization

VI. Conclusion And Future Work

Modern integrated circuit design must incorporate energy-efficient validation due to the increasing need for high-performance semiconductor devices. As ICs scale in complexity and density, managing power consumption during testing phases has become essential not only for ensuring high yield and reliability but also for preserving product integrity and thermal stability. Innovations in Design-for-Testability (DfT) must now transcend traditional functional verification and actively incorporate power-aware considerations. This review examined the key challenges associated with power dissipation during IC testing, including excessive switching activity, scan-induced peak power, and thermal stress. It highlighted a broad range of advanced techniques, including low-power scan architectures, test pattern compression, scan chain optimization, and power-constrained ATPG, all aimed at minimizing both dynamic and static power during test.

Future research should prioritize the integration of AI and ML for adaptive test generation, dynamic power modeling, and real-time optimization. There is a pressing need to develop scalable and thermally-aware DfT methodologies tailored for complex architectures such as 3D ICs, heterogeneous SoCs, and edge devices. Incorporating security-aware mechanisms and context-driven test scheduling will further enhance trust and resilience in modern chip validation. Additionally, emphasis must be placed on real-time power monitoring, on-chip thermal control, and sustainable test frameworks to address evolving environmental and design constraints.

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