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SURVEY ON POWER-AWARE TEST SCHEDULING AND SCAN CHAIN OPTIMIZATION IN SOC TESTING

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Abstract—The growing complexity of System-on-Chip (SoC) designs has heightened challenges related to excessive power consumption during testing, particularly due to high switching activity in scan-based methods. Managing this power effectively is essential to avoid IR-drop, thermal hotspots, yield loss, and long-term reliability issues. This paper presents a comprehensive survey of power-aware test scheduling and scan chain optimization techniques, focusing on reducing both dynamic and static power during testing without compromising fault coverage. It reviews approaches such as time-division, session-based, and thermal-aware scheduling, alongside scan chain reordering, partitioning, multi-chain architectures, and low-transition pattern generation. Design-level techniques, including clock and power gating, and test-level strategies like X-filling, are also discussed. Recent advancements integrating machine learning, heuristic optimization, and adaptive scheduling are analyzed, highlighting their potential for efficient and reliable SoC testing. Comparative insights from literature reveal emerging trends and key challenges. The study emphasizes the importance of combining design- and test-level methods to achieve low-power, cost-effective, and high-yield SoC testing in modern semiconductor manufacturing. Future research can explore AI-driven, real-time optimization frameworks for adaptive power management in complex SoC environments.

Keywords—System-on-Chip (SoC), Power-aware testing, Test scheduling, Scan chain optimization, Low-power testing, Semiconductor manufacturing.

I. INTRODUCTION

Applications in artificial intelligence (AI), the Internet of Things (IoT), medical systems, and embedded computing are powered by System-on-Chip (SoC) architectures, which were made possible by the fast advancement of semiconductor technologies [1][2]. Platforms enable real-time, high-speed performance by integrating storage, computing, and specialized hardware. The term "System-on-Chip" (SoC) refers to a type of hardware platform that allows for effective and practical communication between numerous functional modules. In a standard system on a chip (SoC) [3], you can find a central processing unit (CPU), I/O ports, storage components, DACs, ADCs, and even blocks specifically designed to process signals and images [4]. SoCs are now more complex since they incorporate the concept of several functional blocks and cores onto a single silicon chip. Testing of such complex SoCs becomes a challenge due to the increasing demand for better performance and reduction in power consumption [5].

The conventional testing techniques tend to consume excessive power and occupy more time, which may damage the chip or render it unreliable [6]. Some of the important research areas to address these issues entail the power-aware test scheduling and optimizations related to scan chains. Scheduling tests in a way that limits their peak and average power usage is the main concern of power-aware test scheduling [7]. It maintains control over the timing of tests and test patterns, which can greatly reduce spikes in power that occur when testing a system on a chip. This increases test quality and reduces costs and guarding against damage caused by high switching activity. It is also the core technique of reliable and efficient testing of system on chip.

Power-aware scheduling can be augmented with scan chain optimization, which is dedicated to ensuring that scan chains--serial paths of flip-flops during testing--are arranged to optimize test throughput [8]. Scan chains that are well-structured reduce switching overhead without increasing power consumption or the time required to apply the test [9]. Techniques based on optimisation have been used extensively to optimise scan chain configurations, including scan chain reordering, scan chain segmentation, and scan chain balancing [10]. Optimizing scan chains and power-aware test scheduling work together to create a system that tackles the dual challenges of reducing power consumption and test time in system-on-chip (SoC) testing [11]. The survey presented has emphasised the importance of combining these two methods because it enhances test efficiency and reduces power overhead in the manufacturing of SoC dependably and economically.

A. Structure of the paper

This paper is organised as follows: Section II discusses the issue of power in SoC testing, the sources of power consumption, and the effects thereof. The power-aware techniques of test scheduling are presented in Section III and scan chain optimization techniques are presented in Section IV. In Section V find a literature review of recent developments and in Section VI show its conclusion with key findings and future research prospects of effective SoC testing.

II. POWER ISSUES IN SOC TESTING

System-on-Chip (SoC) systems are becoming more complicated, and alongside them the issues with the power consumption during testing are becoming more important**.** While normal operation typically allows for optimization and control over power, testing often results in power spikes due to increased switching activity, especially in scan-based designs, as illustrated in Figure 1**,** illustrates an SoC test setup with key components (CPU, GPU, Memory, I/O) connected to Automated Test Equipment (ATE). It highlights critical power issues like Voltage Droop, IR Drop, Ground Bounce, Inrush Current, and Excessive Power Consumption, marked by

lightning bolts. These phenomena threaten the device under test (DUT), affecting yield, reliability, and cost. Consequently, managing power during testing is now a vital aspect of design-for-testability (DFT) [12] requiring dedicated power-aware test strategies.

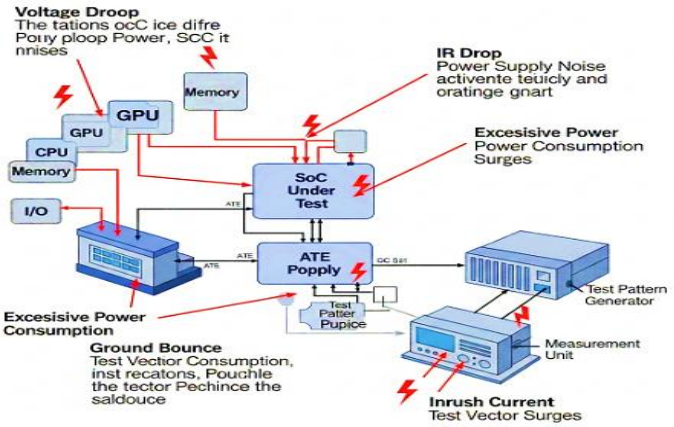

Fig. 1. Power Issues in SOC Testing

A. Test Power Consumption

The average power consumption of a circuit is the sum of all the energy consumed divided by the total time that is taken into account. For the circuit to pass testing, its average power consumption must be within the package's heat dissipation restrictions. Also, from a reliability perspective, it matters because hotspots caused by increased average power consumption might impact the functioning of circuits.

Power spikes during sub-cycle intervals are referred to as instantaneous peak power, while peak power consumption is the maximum power consumed in a single cycle. In most cases, the design of the electrical grid dictates the maximum allowable peak power during testing. One example is a 130 nm ASIC design with 1 M gates and 300 kbits of SRAM working at 150 MHz. According to Texas Instruments, certain transition fault patterns could only pass when the supply voltage exceeded 1.55 V, demonstrating that increasing peak power reduces yield.

B. Sources of Excessive Test Power

Power usage during testing in System-on-Chip (SoC) designs is frequently much higher than during normal operation. Scanning huge amounts of test data across scan chains causes a great deal of switching activity, which is the main cause of this disparity. The main reasons for having too much test power are [13]:

1) Scan Shifting Activity

During scan-in and scan-out operations, numerous flip-flops toggle simultaneously, generating substantial dynamic power due to increased capacitive charging and discharging.

2) Simultaneous Activation of Cores

Testing multiple cores concurrently without power-aware scheduling results in cumulative power that may exceed safe operational limits.

3) Unoptimized Test Patterns

Random or pseudo-random test vectors often lack correlation with functional activity, resulting in higher switching and power dissipation.

4) Test Compression Techniques

Some of the test data compression techniques may usefully decrease switch data but unintentionally raise power by clustering the switching activity into fewer test timeframes.

5) Inadequate Power Gating or Clock Gating

Weaknesses in activation of gating mechanisms during test mode do not quench superfluous switching in idle blocks.

C. Impacts of High-Test Power

The high usage of power when testing SoCs can lead to various negative outcomes, such as IR-drop, thermal problems, loss of yield, and compromise of reliability over time. The most significant ones are the drops in IR-drop and thermal problems together with the loss of yields and long-run reliability problems.

1) IR-drop and Thermal Effects

The power of the test is greater than the power delivery capacity of the SoC, resulting in what is referred to as an IR-drop or a voltage drop through the internal power delivery network of the circuit because of resistive loss. Reduction of voltage may cause timing violations, improper logic assessment and no-pass testing. Besides the effects of voltage, intensive switching activity may cause spot heating which can generate hot zones of thermal activity. The rise in temperature is also harmful to the integrity of the device during a test and may accelerate the aging processes including electromigration and stress caused by the thermal gradient.

2) Yield Loss and Reliability Concerns

SoC devices were subject to permanent damage in high power testing particularly with older density technology nodes where power densities are being explored. Latent defects can activate and burn-in failures to take place involving high power, high temperature and IR-drop drivers can occur, which on the way, may lessen manufacturing yield. In some instances, passing functional tests and subsequent stressing during test conditions may lead to early-life failure and contravene field reliability. Sometimes the most aggressive test conditions that reveal defects, can introduce new faults, creating test overkill and running good units.

The risks highlight the importance of using power-aware test approaches to protect device performance, device yield, and overall product reliability in contemporary SoC production.

III. Power-Aware Test Scheduling Techniques

System-on-chip (SoC) testing requires power-aware test scheduling, and the test process must be optimized to use as little power as possible so that damage from normal high switching activity is prevented. Good test scheduling methods maximize the test coverage subject to power limitation conditions, making it safe and economical testing [14]. The power constraint test schedule algorithm is all about creating an optimum test schedule graph (TSG) whilst maintaining the maximum power threshold limit of the SoC. Figure 2 shows that this process starts with generation of core characteristics, which is followed by determining the Modified SoC (MSoC) meeting the power restriction. The weight to each node in MSoC is assigned, and the initial TSG is developed. The algorithm next converges over incomplete nodes with a sequence consisting of: adding potential Built-In Self-Tests (BIST) nodes, creating new deterministic test patterns (DTPs) from partial response test patterns (PRTPs), and finetuning weights. Until these nodes are complete, this cycle is repeated until a final optimized TSG is achieved which ultimately balance test efficiency and power constraint in SoC testing.

```
Inputs: 1) core characteristics (SoC)
        2) Maximum power limit (Pmax)
Output: Optimal test scheduling graph (TSG)

Test_Scheduling(SoC, Pmax)
1  core_characteristics = test_generation(SoC);
2  MSoc = Finding MSoC(core_characteristics, Pmax);
3  Weighted_MSoC=Assign a weight to each Nk set in
   MSoc;
4  TSG = scheduling_TSG(Weighted_MSoC);
5  WHILE (there is incomplete node in TSG)DO
6    Add possible BIST part to each incomplete node;
7    Generate new DTPs for based on added PRTPs;
8    Weighted_MSoC=Assign a weight to each Nk set in
     MSoc;
9    TSG = scheduling_TSG(Weighted_MSoC);
10 END
11 RETURN TSG;
   END
```

Fig. 2. Algorithm for Power Constraint Test Scheduling.

A. Test Scheduling in SoCs

Modern System-on-chip (SoC) designs involve a delicate balance of power and time constraints and cost requirements in test. The architecture of the majority of modern SoCs is modular with each core or functional block being designed, optimized and tested in isolation. This has the advantage of flexibility and the ability to use low power test techniques specific to individual modules but it also introduces difficulties in putting together a productive total test plan in the context of the chip as a whole [15].

A common strategy to test power control is single-module testing where a single module is powered and the rest maintained in a constant or idle condition. It is low overhead switching and energy efficient, and the disadvantage is the total test application time is longer than the case with little use of dynamic power, which may add cost to the manufacturing operation. The other method is parallel module testing where several modules are tested at a time in order to reduce the total test length. Although this provides an efficiency, it may result into transgression of power limits in case low-power management traits are not portable in the scheduling process. IR-drop, localized heating and even functional failures during testing can be produced by excessive simultaneous activity.

This problem can be transformed to be more complex in those heterogeneous SoCs where it combines a varied processing elements like CPUs, GPUs, DSPs and even hardware accelerators. The power profile, scan chain architecture and other resource requirements can be quite different among these components and thus come up with a test plan that meets power and bandwidth requirements. To overcome these issues, power-constrained test scheduling techniques have been devised, aimed at maximizing the time during which tests are run, and at enforcing power consumption per time instant to be within some sensible parameters associated with safe operation of test systems or power systems.

B. Power-Constrained Test Scheduling Methods

Power-constrained test scheduling methods focus on minimizing test time while ensuring that instantaneous power consumption remains below a given threshold. These methods can be broadly categorized into **time-division**, **session-based**, and **thermal-aware** scheduling techniques.

1) Time-Division Test Scheduling

Like dynamic test scheduling methods, time-division test scheduling divides the total test process time into a number of time slots with a different allotment of cores made in each time slot such that power during said time slot does not exceed the designated limit [16]. Time-division test scheduling satisfies the design requirement of always being under the budgeted power limit, however, it could ultimately result in higher test time. Time-division methods are typically fairly easy to carry out, and they are a good option when the test power used at different cores is substantially different.

2) Session-Based Test Scheduling

Session-based scheduling divides test time into test sessions, each consisting of a subset of cores tested in parallel. Session-based scheduling can be considered a more flexible version of time-division scheduling as it allows to choose which cores are grouped together based on power and other resource limitations [17]. Each session is developed in such a way that ultimately both the total power and resource usage (e.g., TAM width, scan bandwidth), remain under the bounds allowed. Integer Linear Programming (ILP), Constraint Programming (CP), and Evolutionary Algorithms (EA) are popular techniques for finding the best or near best test sessions.

3) Thermal-Aware Scheduling

Thermal-aware scheduling extends power constrained scheduling with regard to the thermal profile of the SoC during testing [18]. Even concerning the global power budget, excessive localized heating can occur, causing thermal hotspots to emerge on the SoC. For thermal-aware scheduling to work effectively, the heat distribution from the cores over the entire chip must be modeled, and scheduling tests to avoid or reduce hotspots follows from that model. The approach normally includes staggering the tests of high-power cores and incorporating cooling time between testing a large number of cores. Some approaches begin to rely on thermal simulation or temperature estimation models, which may provide a means of dynamically guiding the scheduling to mitigate the hotspots.

C. Resource-Constrained Test Scheduling

In modern SoC designs, the growing number of cores, IP blocks, and functional units enables high levels of parallel testing. This parallelism has its own limitations in terms of shared resource limitation like the bandwidth of the test access mechanism (TAM), the number of Automatic Test Equipment (ATE) channels, on-chip test data storage capacity, and power delivery capabilities. Resource-limited tests scheduling is a test optimization technique that seeks to identify the best combination and order of the fundamental tests of scheduling to ensure that any resource is not overcommitted and hence results in lack of performance or reliability concerns [19]. Common constraints are narrow bandwidth within TAM due to contention with multiple cores under test, limited ATE channels offering simultaneous scan input and output, on-chip memory used to store built-in self-test (BIST) or compressed tests, and low power budgets due to the inability to turn on multiple high-power cores in parallel to meet the constraints on IR-drop and thermal IR-drops and thermal violations.

Scheduling generally takes the form of a combinatorial optimization problem. To optimize on total test application time (TAT) but with all the resource constraints met, heuristic methods like greedy search, simulated annealing and genetic algorithms are usually employed alongside exact methods like Integer Linear Programming. Resource constrained test scheduling has the capability of optimally using the resource in the hardware, allow scalability of testing of large SoCs and can be adapted to meet physical constraints set thus the production cost is kept lower without compromising on the quality of testing.

The strategies pave the way to other advances in test efficiency through the allowance of greater correspondence between test delivery mechanism and the supporting hardware architecture.

IV. Scan Chain Optimization Techniques

Scan chain optimization plays highly significant role in minimizing power, test time and area overhead of the testability of System-on-Chip (SoC) designs [20]. Figure 3 replaces the circuit shown in Figure 1 by a design of the Digital Circuit up to 4 possible ways of enhancing testability. Techniques such as Chain Reordering focus on rearranging scan cells to boost test throughput, while Scan Cell Grouping aims to shorten the scan chain length. The diagram also highlights Test Point Insertion and Test Point Optimization, which help minimize clock domains and reduce overall test duration. Additional strategies including Clock Domain Optimization, Partial Scan, and Clock Domination are illustrated, all contributing to better management of clock signals and scan chains to enable power-aware test scheduling and improved test coverage.

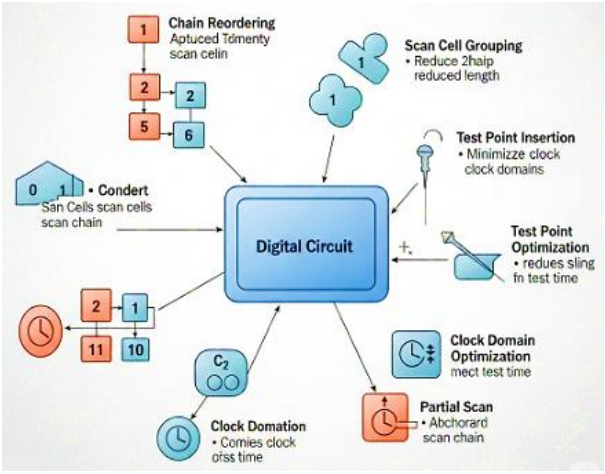

Fig. 3. Scan Chain Optimization Techniques

A. Scan-Based Design-for-Testability (DFT)

Scan-based DFT is a very common approach used in digital VLSI design to improve testability. In this technique, it can replace or complement standard flip-flops with flip-flops that can-do scan (i.e., scan flip-flops), allowing us to construct a scan chain. The internal nodes of the circuit may be controlled and observed during testing thanks to a scan chain, which allows test data to be shifted serially into and out of the circuit [21]. While improve fault coverage and reduce the difficulty of test generation with scan-based DFT, scan-based DFT introduces additional complexity particularly in the areas of test power, scan routing overhead, and test time. If don't target some of these issues and optimally design a scan architecture, the scan operation may toggle flip-flops at higher frequencies resulting in higher dynamic power dissipation.

B. Power-Aware Scan Chain Design

Power-aware scan chain design aims to minimize the dynamic power consumed during scan shifting by reducing switching activity and balancing scan chain lengths. Scan chains for low-power testing can be optimized using a number of different methods.

1) Scan Chain Reordering

Rearranging scan chains switching up the flip-flop sequence in the scan chain so that scan-shifting is as smooth as possible. If flip-flops with high logic correlation or low switching activity are placed close to one another, the total toggling across the scan chain can be reduced significantly [22]. It can involve algorithmic formats like a Traveling Salesman Problem (TSP) heuristics or graph-based clustering, where the flip-flops are ordered such that the Hamming distance between the next state and the present state turns out to be minimized. Reordering reduces peak power during scan and can help avoid voltage droops and false test failures.

2) Scan Chain Partitioning

The process of scan chain partitioning involves slicing a lengthy scan chain into numerous smaller pieces. During each scan shift cycle, only a subset of scan chains is active, while others remain idle or gated, thus reducing instantaneous switching activity. Partitioning can be static, with fixed scan subsets, or dynamic, where partitions are activated in a time-sliced manner. This approach effectively spreads out the switching events over multiple clock cycles, lowering peak power density and easing power delivery constraints. Moreover, partitioning facilitates localized testing, especially in modular SoC designs, enabling core-level scan control and power management.

3) Multi-Scan Chain Architecture

In a multi-scan chain design, numerous scan chains run in parallel, cutting down on the length of each scan chain and the number of clock cycles needed for scan shifting. Although this reduces test time, this architecture can result in more concurrent switching if not properly controlled [23]. To attempt to make power-aware a multi-scan chain architecture, balanced scan insertion, low-transition pattern generation, and segment gating have been described as usages to avoid excessive power. Dynamic power balancing of multiple scan chains is one approach to ensure that no single scan chain drains the power budget. Multi-scan chains can be very useful for large SoCs where reduced test time is critical, and power must still be met.

4) Low-Transition Pattern Generation

This technique creates test vectors to decrease dynamic power consumption by reducing the number of bit transitions between successive patterns. By assigning values to "don't care" bits, techniques like X-filling make testing more reliable and efficient while also limiting toggling and ensuring balanced power distribution.

Overall, power-aware scan chain design effectively reduces switching activity and dynamic power during testing, laying a strong foundation for further low-power strategies.

C. Power Optimization Techniques

Power optimization is a critical aspect of modern digital circuit design and testing, aimed at minimizing power consumption to improve energy efficiency, reduce heat generation, and enhance device reliability. The two main types of power are dynamic power, which results from switching operations, and static power, which is the result of leakage currents. Below, the outline the two main categories into which the offered approaches fall: design-level and test-level.

1) Design-Level Techniques

Design-level techniques focus on reducing power consumption during normal circuit operation by optimizing the hardware architecture and control mechanisms.

- **Clock Gating**: Among the several dynamic power reduction techniques, clock gating is among the most common. In order to stop unused switching activity in idle functional blocks or registers, it disables the clock signal to those components [24]. By selectively gating the clock, the switching activity—and consequently

dynamic power consumption—is significantly reduced without affecting the functionality of active blocks.

- **Power Gating**: Clock gating and power gating work hand in hand to minimize static power, often known as leakage. For this purpose, it uses sleep transistors or power switches to disable blocks that are not actively processing data. Thanks to power gating, leakage current is significantly reduced when a module is not in use by turning off its power domain.
- **Dynamic Voltage and Frequency Scaling (DVFS)**: DVFS is able to sense the current load and adapt the circuit's supply voltage and clock frequency accordingly. When there is little activity, lowering the voltage reduces power consumption quadratically, while lowering the frequency reduces power consumption linearly. Here, they find a happy medium between power savings and performance requirements.

2) Test-Level Techniques

The power used in a test may be a lot more than when the device is operating normally because of the more switching that takes place and therefore causes reliability problems and test escapes. Techniques which do test application at test level achieve minimum power application without affecting fault coverage.

- **Scan Chain Reordering**: Reduce the amount of bit transitions caused by moving scan data around in the scan chain by reordering the sequence of flip-flops within the scan chain, as is done in scan-based testing. Reduces transitions also resulting in reduced dynamic power consumption during test, which should be lower than during use to limit the chance of overheating and damage.
- **X-Filling (Don't-Care Bit Filling)**: During test pattern, don t care bits (Xs) are frequently found and explicitly replaced with 0s or 1s to reduce switching activity between consecutive test vectors. Through X-filling optimization of toggling is minimized in combinational logic and thereby reduces the amount of power consumption during test.
- **Test Scheduling Under Power Constraints**: Test scheduling algorithms partition the total test into use sessions or Time windows so that the instantaneous power dissipation does not violate specified limits. Ensuring such control over the order and the concurrency of the test application, these techniques eliminate excessive power spikes and thermal stress.

Reducing power consumption and improving the efficiency and reliability of digital circuits during operation and testing can be achieved by combining power optimizations techniques at the design and test levels.

V. LITERATURE REVIEW

This literature summary highlights diverse advancements in power-aware SoC testing, including machine learning-based estimation, scan chain optimization, energy management, and fault diagnosis. The studies address key challenges in power efficiency, scalability, and real-time implementation across varied application domains.

Haraz et al. (2025) a thorough method for estimating EV LiBs on-chip using machine learning (ML), which takes into account uncertainty, real-world data variability, and model dependability. Preprocessing techniques, such as scaling and normalisation, were used in conjunction with rigorous cross-validation approaches to guarantee the model's resilience and generalisability. All of these steps were integrated into a well-structured ML pipeline, which improved the overall efficiency and usability of the model creation cycle [25]

Vartziotis (2025) A user-friendly system for industrial testing, the TDM Test Scheduler and TAM Optimisation Toolkit is presented in this study. It is designed for engineers, researchers, and teachers. The toolkit enables test planning for multicore, DVFS-based systems on chips with different voltage islands, and it offers optimised solutions that reduce test expenses while guaranteeing compliance with power and thermal constraints. It has a high-level language, a clever logic and grammar checker, a sophisticated environment for compilation and execution, a framework for optimising TAM, a customisable environment for visualisation, and a flexible testbed for research and education [26]

Antony et al. (2024) a method for improving scan chain wirelength employing hierarchical clustering through the use of single linkage and geometry-based balancing to meet test criteria. For specific topologies, the suggested technique outperforms the widely used K-means clustering method by as much as 10%. Rearranging the connections between scannable elements in a physical design flow called "scan chain optimizations" shortens the overall wirelength, which improves routing capabilities and power [27].

Kim et al. (2023) A new hardware architecture that duplicates data is suggested for the purpose of fault location diagnosis through intentional voltage collision, regardless of the number of faults that may occur. A diagnostic line, a diagnosis circuit, and at least one good scan chain are necessary resources for the diagnosis. The experimental results show that the proposed method is superior to the existing one in terms of hardware and routing overhead, additional pin counts, and overall performance. As the number of scan chains (circuit size) rises, the diagnostic time is increased and the diagnostic performance is improved compared to older procedures [28].

Habiby, et al. (2022) developed the IJTAG method to address the increasing complexity of system-on-chips by focusing on reconfigurable scan network–based efficient access techniques. This approach shortens scan chains, which in turn saves test time, without lowering test quality. For the IJTAG approach to work with newer designs of multi-power domain chips, a test scheduler that takes into account the limitations of specific instruments is essential. This research presents two new methods for scheduling tests that take power considerations into account. These techniques utilise numerical linear programming and pseudo-Boolean optimizations. One method determines the optimal time to conduct tests on networks with over a thousand devices, while the other optimizes the execution of tests on networks of medium size [29]

Priya and S (2021) explore the growing trend of VDSM technology in VLSI, which is propelling the development of smaller, more powerful, battery-operated smart computers. Design and test engineers must prioritise power minimisation, and testing these devices should take hierarchy levels into account at different phases. In this study, compare heuristic methods for reducing scan power through X-filling with methods for creating bounds for industrial performance tests utilising ISCAS'89 Benchmarking circuits. Compared to standard scan operation, the suggested method can cut power consumption by 70%; the novel method can reduce power consumption by up to 63.62 per cent on the shift component and 69.9 per cent on the capture component; and the X-factor can be as low as 0.57 [30]

Table I presents a comparative summary of recent studies on power-aware test scheduling and scan chain optimization in SoCs, highlighting diverse methodologies, key findings, challenges, and future research directions

TABLE I. LITERATURE SUMMARY ON POWER-AWARE TEST SCHEDULING AND SCAN CHAIN OPTIMIZATION IN SOC TESTING

Author	Study On	Approach	Key Findings	Challenges	Future Directions
Haraz et al. (2025)	ML-based SoC estimation for EV LiBs	Machine learning with normalization, scaling, and cross-validation in a structured pipeline	Robust and generalizable model for SoC estimation under real-world variability	Handling uncertainty and ensuring reliability in diverse data	Enhance ML integration for real-time, adaptive power-aware scheduling in SoC environments
Vartziotis (2025)	Optimization Toolkit for TAM and TDM Tests	Multicore DVFS-based system on a chip (SoC) development kit with integrated tools for multiple voltage islands, HLL, TAM optimizations, and testbed	Supports power- and thermal-aware test planning; minimizes test costs; user-friendly for research and industry	Adapting toolkit for larger and more heterogeneous SoC designs	Extend toolkit for AI-driven dynamic scheduling and TAM adaptation
Antony et al. (2024)	Scan chain wirelength optimization	Hierarchical clustering (single linkage) with geometry-based balancing, compared with K-means	Achieved ~10% wirelength reduction; improved routability and power efficiency	Adapting to different design topologies; balance between clustering and design constraints	Develop dynamic scan chain optimization strategies compatible with real-time layout changes
Kim et al. (2023)	Fault diagnosis in scan chains	Hardware architecture with data duplication and voltage collision for multi-fault diagnosis	Lower hardware/routing overhead, faster diagnosis, scalable with scan chain count	Ensuring diagnosis accuracy with minimal resources	Adapt method for low-power, high-speed test scenarios in SoCs with large scan chains
Habiby, et al. (2022)	IEEE 1687 (IJTAG) power-aware scheduling	Transformable scan networks optimized for multi-power domain systems on chips using pseudo-Boolean and ILP techniques	Reduces scan chain length & test time while avoiding IR drop; scalable to large networks	Overhead from network reconfiguration	Integrate machine learning for adaptive IJTAG scheduling
Priya and S (2021)	Scan power reduction	X-filling heuristic vs. industrial test bound techniques using ISCAS'89 circuits	Up to 70% power reduction; significant reduction in shift/capture components	Integration into industrial ATPG flows	Apply X-filling to multi-power domain SoC testing

VI. CONCLUSION AND FUTURE WORK

Effective management of test power in System-on-Chip (SoC) designs is essential for maintaining yield, reliability, and performance in increasingly dense and heterogeneous architectures. Excessive switching activity during testing can cause IR-drop, thermal hotspots, and reduced device lifespan, making power-aware strategies critical for ensuring safe and efficient testing. Techniques such as time-division, session-based, and thermal-aware test scheduling help balance concurrency with power limits, while scan chain optimization methods—like reordering, partitioning, and low-transition pattern generation—significantly reduce dynamic power. A complete reduction of static and dynamic power can be achieved by combining these with design-level power reduction techniques such as power gating and clock gating. The literature also highlights a shift toward AI-driven, adaptive testing solutions capable of real-time scheduling, predictive power management, and context-aware optimization, making them highly relevant for next-generation SoCs.

The integration of adaptive test scheduling frameworks that utilize machine learning and artificial intelligence to dynamically control power during system-on-chip (SoC) testing should be the focus of future study. Incorporating lightweight thermal modelling and selective resource-aware strategies will further enhance testing efficiency. Linking hardware-level improvements with adaptive scheduling will continue to improve cost-effectiveness, reliability, and scalability, supporting sustainable semiconductor manufacturing in the Industry 4.0 era.

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