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A Low Power 27.4GHz Differential LC Oscillator using 45 nM in submicron Technology

Prof. Dr. S. V. Rode
Electronics & Telecommunication Dept.
Sipna C.O.E.T,
Amravati, India

B. R. Mankar*
Electronics & Telecommunication Dept.
Sipna C.O.E.T,
Amravati, India

Abstract: A CMOS differential LC Oscillator is investigated, which is capable of operating at millimetre- wave (MMW) range with low dc power consumption. Very few CMOS in LC Oscillator are also used. The differential LC Oscillator is demonstrated through 26 GHz integrated LC Differential Oscillator implemented in Microwind's CMOS 0.45 nm-High K/Metals – 3rd generation Strain-8 metal copper process. The oscillator uses one inductor, two capacitors, two NMOS and two PMOS as its tank circuit. With core power consumption of 0.297mW at 27.0^{0}C. This Differential LCO is believed to have the best figure of merit among MMW LCO's suing bulk CMOS process.

Keywords: CMOS, LC Tank, Differential oscillator, Design methodology, Phase Noise.

I. INTRODUCTION

The first oscillator configurations using vacuum tubes were based on the electromagnetic Coupling between the output and input circuits. In this case, the oscillation frequency is approximately equal to the resonant frequency of the parallel LC circuit if the coupling and active device parasitic are small enough. To realize a phase balance condition in the Feedback-coupled oscillator, the Feedback should provide a phase shift of 180◦. [2]

Many papers and books suggest that the differential LC oscillator is the most preferred oscillator for RF systems as it has lower phase noise compared to other oscillators [3, 4]. The LC Oscillator topology needs fewer active devices that could increase the device noise within the oscillator. LC oscillators are based on the resonant effect of the passive inductor and the capacitor in the circuit. The basic topology of the cross-coupled LC oscillator has two PMOS transistors and two NMOS transistors. They are differential to each other with the respective output signals having equal amplitude and are 180^0 out of phase. This oscillator is not symmetric, so the harmonics are significant. Phase noise can be reduced by making the layout of the oscillator symmetric [5] and by increasing the quality factor (Q) of the tank circuit.

II. THE OSCILLATOR DESIGN

Nowadays, thanks to technology scaling, mm-wave circuits can be designed in CMOS. But in those CMOS technologies the reduced supply voltage is a major design challenge for low Phase-noise oscillators. To cope with this issue at GHz frequencies, [7] has proposed an enhanced LC tank using bond wire inductors. But when moving to 50 GHz, those techniques become difficult and at least four design challenges arise: The first challenge comes from the high operating frequency. The second challenge is the low varactor quality factor up to 50GHz. The two parameters important for a varactor are the tuning ratio and the quality factor (Q). The third challenge is related to the tuning range. To achieve a certain tuning range, the maximum and minimum values of the tank capacitance should meet a certain ratio:

$$\gamma = \frac{C_{v\,max} + C_p}{C_{v\,min} + C_p} = \frac{1+\alpha+\beta}{1+\alpha-\beta} \quad (1)$$

Where, Cv is the varactor capacitance and Cp is the parasitic capacitor, that includes the capacitance form transistor in cross-coupled pair and buffer stage inductor and interconnect line where the parasitic capacitance is parallel with the varactor capacitance ($C_{vmax} \leq C_p \leq C_{vmin}$).

Where as parameter are representing the varactor tuning ratio and the ration of parasitic to varactor capacitance resp. According to (1), the tuning range can be increased either by increasing or by decreasing [9] by reducing the capacitive loading from buffer stage or by increasing the varactor value can be reduced. But by reduction of capacitive loading that results in the less output power. To increase the output power, an additional output power stage is should be added but that results in the unwanted DC power consumption. Similarly by increasing varactor value can be increases that decreases the tank impedance, to avoid that condition transistor with large Negative resistance will be needed, otherwise the oscillations will not be started. Also increasing the varactor value will deteriorate the tank quality factor Q-tank, thus that causes the increase of the phase noise according to the lessons formula. [8] The fourth challenge is to keep the very large oscillator gain (Kvco) and the worst reactive linearity. The large Kvco is caused by a tuning range in a low supply voltage.

Figure 1: illustrate the Schematic diagram of Differential LC Oscillator. Very few NMOS & PMOS are used to complete the structure. But important component to design is Tank circuit, specially the Inductor & Capacitor which operate at the 0.5 V as a core voltage. This Lc Oscillator has a differential output whereby two output frequencies produced by tank circuit which has a phase shift of 1800 with each other. When one of the outputs has high potential while at the same time other has low potential.

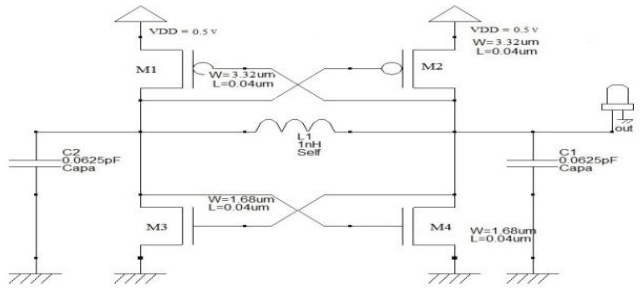

Figure 1: Schematic diagram of Differential LC Oscillator.

The tank circuit uses a triple turn symmetrical octagonal inductor with nominal inductance of 1 nH. Quality factor of the inductor is estimated at 16. The width of the inductor metal lines is kept at 15 pm with metal thickness of 3.2 pm. The tank capacitors are stacked metal finger capacitors with capacitances of 1.0 pF and a quality factor of over 200. Since the Q of the inductor is much smaller than the Q of the metal finger capacitor, the Q of the inductor limits the overall Q of the LC oscillator. The waveforms produced by both the Node are not exactly symmetric where one of Node has higher potential than other this is because layout of the circuit is not symmetric. Assume that the transistors used are ideal transistors.

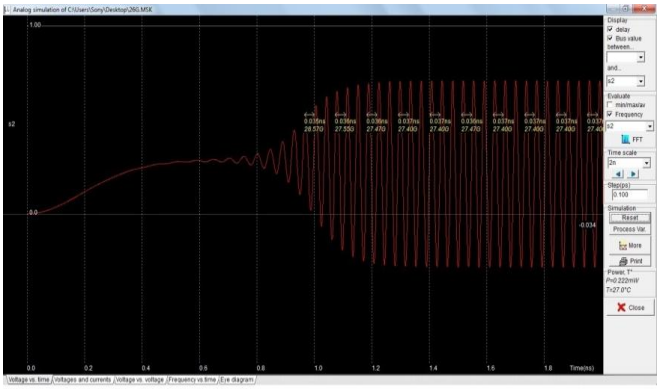

Figure 2: Simulated Output Waveform

From Figure 2: Simulated output waveform shows because of the position where transistor M2 and transistor M3 are in their triode or linear region transistor while Ml and transistor M4 are in their saturation region. Hence, voltage will be pulled up by transistor Ml to VDD and node B will be pulled down by transistor M4 to VSS. The voltage will gradually increase because of capacitor and voltage will gradually decrease. At the same time, current will use the path through the inductor and will energize it. Current flow will continue to rise in the direction of inductor to capacitor through the inductor until the voltage across inductor reaches to 0.55 V. At this point when voltage across the inductor is at 0.55 V, all of the transistors are in their saturation region. Inductor current has reached its peak and starts charging the tank capacitors. Inductor current decreases slowly until node voltages across the inductor reach the next phase. Voltage at node will be pulled up till it reaches near VDD by M2 and node will be pulled down to near VSS by M3. Consequently, transistor Ml and transistor M4 now operate in their respective triode regions while transistor M2 and transistor M3 are saturated. The saturation state directs the transistor M2 to pull node down again to VSS and transistor M3 will pull node to VDD. The different voltage potential between the two nodes of the inductor will start energizing the inductor up again but current flow is now in the opposite direction. Again, inductor current will start dropping the moment both the node voltage across the inductor reaches 0.55 V, to charge up the tank capacitors. This will go on until nodes return to its initial condition. The process will repeat to produce a constant oscillation.

III. RESULTS & DISCUSSION

The circuit has been simulated over process, voltage and temperature and variations (PVT). As shown in Figure 2, this shows us the constant frequency of 27.40 G simulated at standard temperature 270C. The circuit simulation takes very short delay time of 1.3 ns to regulate the operating frequency up to 27.40 G.

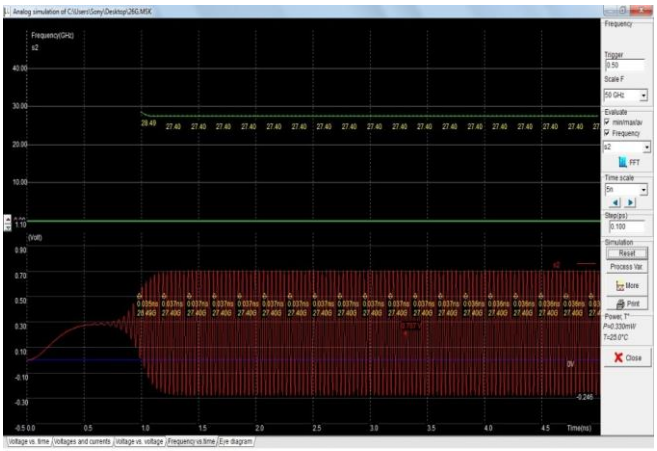

Figure 3: Frequency Vs Time Plot

Figure 3: depicts the oscillation frequency over a range of time up to 5ns. Simulation results show that oscillation frequency is relatively immune to different temperatures but increasing temperature reduces the oscillation frequency accuracy. If the temperature increases the variation in the output frequency increases. The Parasitic from the interconnect wires are carefully included during simulation since interconnect parasitic could reduce the oscillation frequency by as much as 10-20% [6]. The 'max' process comer means the RF transistors used have lower threshold voltage and higher saturation current than the nominal process corner. The 'min' process comer means the RF transistors used are with higher threshold voltage and lower saturation current than the nominal process corner. The 'nominal' process comer has a threshold voltage 0.33 V for the n-type transistor and a threshold voltage of 0.35 V for the p-type transistor. Nominal saturation current density for the n-type and p-type transistor are 535 µA/µm and 235 µA/µm respectively up to 7ns it provides the waveform of voltage rise up to 0.3 V. Initial variations are between the 28.57 G to 27.47 G, but after 1.3ns it takes stable output of 27.40G. the contents and import your prepared text file. You are now ready to style your paper.

Table I. Recent fundamental oscillation frequencies obtained

	Fundamental Frequency	**Power Dissipation**	**CMOS Technology**	**Fundamental Frequency**
[10]	5 GHz	12mW	130 nm	[10]
This Work	27.4 GHz	0.22mW	45 nm	This Work

Table II is comparison made between the Differential LC oscillators implemented using two different technologies (130 nm and This Work (45nm)).

Table 2. Differential LC Oscillator comparison between two different technologies

	45 nm	130 nm
Phase Noise	√	X
Quality Factor	√	X
Power Supply Variation	√	X
Temperature Variation	√	X
Area	√	X

For the 45 nm technology, 8-Metal layer inductors have lower material resistivity up to R=6.50 to 64.58Ω compared to copper inductors in the 380 nm technology. Also, the 450 nm inductors are designed to be thicker than the 130 nm inductor. Thicker metal lines have lower series resistance and thus higher quality factor up to 0.73 to 7.28. Higher Q for the inductor means higher Q for the tank circuit.

Hence, the 45nm oscillator design is expected to have less phase noise and higher quality factor compared to the 130 nm oscillator. 8-Metal layer is also expected to have better voltage and temperature coefficients, therefore this leads to better power supply and temperature immunity for the 45nm LC oscillators. The 45nm chip is also smaller in size since the technology used has smaller dimensions.

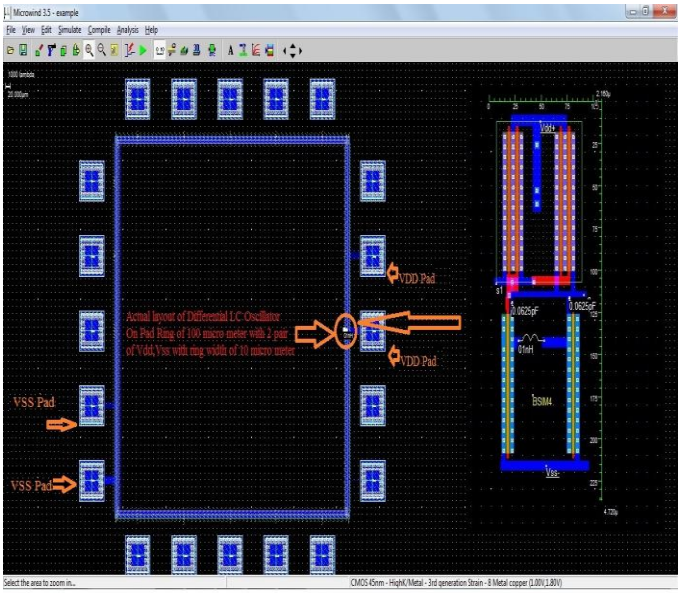

Figure 4 : Layout of Differential LC Oscillator with padding on the actual Die

Figure 4 portrays the layout of the differential cross coupled LC oscillator to be fabricated in the 45nm technology, that has actual size on die is 4.720µm*2.160µm.

IV. CONCLUSION

A differential LC oscillator was successfully designed and simulated using Microwind's CMOS 0.45 nm-High K/Metals – 3rd generation Strain-8 metal copper process CMOS technology. The simulated oscillator frequency is 27.4 GHz at the nominal process corner. The oscillator frequency shows very little dependence to temperature which has very low power consumption & core voltage.

V. ACKNOWLEDGMENT

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VI. REFERENCES

[1]. Ping-Chen Huang, Ming-Da Tsai, George D. Vendelin, Huei Wang, Chun-Hung Chen and Chih-Sheng Chang, "A Low-Power 114-GHz Push–Push CMOS VCO Using LC Source Degeneration",

[2]. Grebennikov, "RF and Microwave Transistor Oscillator"

[3]. Bemy A. D., Niknejad A. M. & Meyer R. G. 2003, "A wideband low-phase-noise CMOS VCO" Custom Integrated Circuits Conf: pg: 555-558.

[4]. Laute A., Peter J. & Teichmann P. 2004, "Designing a low-noise VCO", Microwave & RF.

[5]. Ahrens T., Hajimiri A. & Lee T. H. 1997, "A 1.6 GHz 0.5 mW CMOS LC Low Phase Noise VCO using bond wire inductance" (Online) http://wwwsmirc .stanford.edu/ papers/ cancun97p-tam.pdf (23 March 2005).

[6]. Lim Q. S. I., Kordesch A. V. & Majlis B. Y., "The Effects of Interconnect Parasitics on a 2.4GHz RF LC Oscillator Design", NSM2005

[7]. J. Craninckx and M. Steyaert, "A CMOS 1.8 GHz low-Phase-noise voltage-controlled oscillator with prescaler," IEEE ISSCC Dig. Tech. 1995, pp. 266–267, 377.

[8]. Lianming Li, Patrick Reynaert, Michiel S. J., Steyaert, "Design and Analysis of a 90 nm mm-Wave Oscillator Using Inductive-Division LC Tank", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 7, JULY 2009.

[9]. C. Cao and K. K. O, "Millimeter-wave voltage-controlled Oscillator in 0.13 µm CMOS technology," IEEE J. Solid-State Circuits, vol. 41, no.6, pp. 1297–1304, Jun. 2006.

[10]. Mohd. Shahrul Amran , Queennie Lim Suan Imm, Albert Victor Kordesch, "Design of a 130nm CMOS Differential Cross-oupled 5 GHz LC Oscillator", December 20-21, 2005, Johor Bahru, Johor, MALAYSIA.

Short Bio Data for the Authors

Sandeep Vinayakrao Rode received master's degree in 2004 and PhD in 2014 in Electronics Engineering from Sant Gadge Baba Amravati University, Amravati, India He has 17 years of teaching experience and presently working as Professor at Sipna college of Engineering and Technology, Amravati (India). His main research interests include signal processing, image processing, circuit design etc. He is a member of IEEE, IETE, IE and ISTE. He has published 16 papers in National and International Journal and conferences.

Mr. Bhushan Ruprao Mankar received his bachelor degree from Amravati University, in 2010 & has 1 year experience in Telecommunication industry. Presently he is pursuing Masters Degree in Digital Electronics from Amravati University. His main area of interest is CMOS-VLSI Design challenges, Signal processing etc.