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STUDY OF PARALLEL COMPUTING STRUCTURE AND CIRCUIT ANALYSIS FOR INTERCONNECTION NETWORK

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Abstract: Parallel computing has become a crucial topic in the concern of computer science and also it is revealed to be critical when researching in high performance. The evolution of computer architectures towards an improved number of nodes, where parallelism could be the approach to option for speeding up an algorithm within the last few decades. The combination of processing units build a model of computation (circuits) has gained an essential place in the area of high performance computing (HPC) due to its configuration and considerable processing supremacy that is parallel, series, etc…. In this paper, we study the idea of parallel computing, and its programming models and also explore some theoretical and technical concepts which can be often needed to understand the Interconnection network. In particular, we show how this technology is new in assisting the field of computational physics, especially when the issue is data parallel. In this paper firstly we convert the graphical model of perfect difference network into circuit diagram then convert circuit diagram into switching function, then simplify it and redraw the equivalent network.

Keywords: Circuit analysis, Boolean function, High performance computing, Interconnection Network

INTRODUCTION

Parallel computing systems offer the promise of a quantum leap in the computing power that can be brought to bear on many important problems[1]. The reason for parallel computing is dependable to develop an application execution by playing out the application frame sort on various processors. While parallel computing is usually for High Performance Computing, it's becoming more prevalent in the mainstream computing as a consequence of the present growth of commodity architecture called multiprocessor[2, 3]. The study of parallel structure of perfect difference network shows the circuit and robustness of the Perfect difference network. Certain applications of computers require much more processing power than can be provided by today's machines. These applications include solving differential equations and some areas of artificial intelligence like image processing. Efforts to increase the power of sequential computers by making circuit elements smaller and faster have approached basic physical limits4. Consequently, it appears that substantial increases in processing power can only come about by somehow breaking up a task and having processors work on the parts independently. The parallel approach to problem-solving is sometimes very different from the sequential one. To convey these situations we may use alternate or mixed pattern. In this paper, we have discuss the concept of topological properties, study the structural relation of perfect difference network(PDN) architecture.

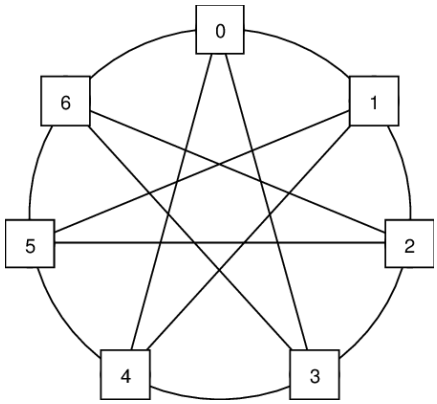
PARALLEL STRUCTURE AND CIRCUIT ANALYSIS ON PERFECT DIFFERENCE NETWORK

An interconnection network of futuristic computer systems fully exploits the computational power of processing elements[4]. In this research work perfect difference network can be modeled using graphs. The nodes of the graphs are as processing element and the nodes are connected by graph edges known as communication arcs. An abstract graph structures are important to find the structural relationship in interconnection network[5, 6]. The real life interconnection network systems modeled as graph can be analyzed for its algorithmic complexity by implementing graph theory combined with theory of matrices. Presently, upcoming high speed interconnection networks such as perfect difference network (PDN) had been successfully studied by a Prof. Rakesh Kumar Katare, and his research group for its topological properties[7, 8, 9].

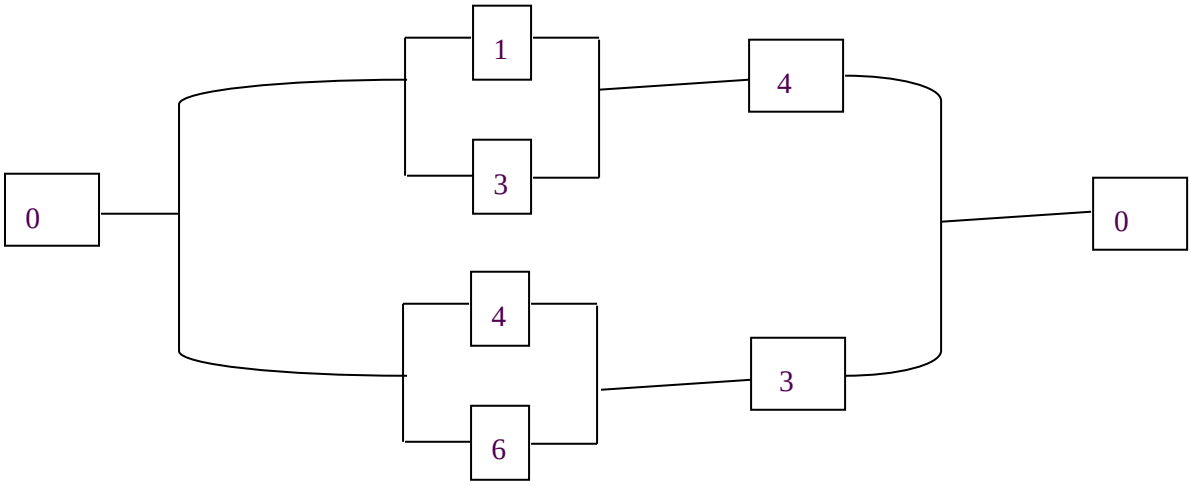
There are two main aims

1. Elaborate parallel communication structure in PDN.
2. To convert parallel structure into parallel expression

The parallel expression of PDN enables the architect to enhanced degree of parallelism in communication and to reduce processing time in most simple form[10].



We have studied the interconnection network PDN with δ=2, having $\delta^2+\delta+1$ nodes. We assume *c* is the number of distinct circuits and *e* is the number of communication arcs represented as edges of PDN graph model G. PDN has $\delta^2+\delta+1$ nodes, then the communication function is denoted by $C(\delta^2+\delta+1)$ Here we elaborate the parallel structure starting from node 0; The circuit diagram will be as follows,



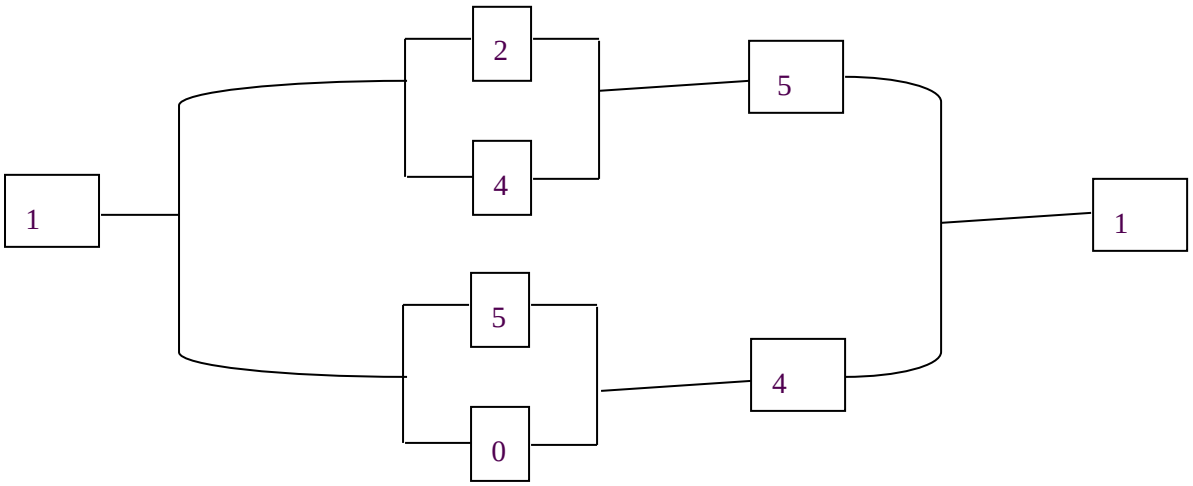
0^ (1V3) and 0^ (4V6) both are in parallel and 0 ^ (1V3) are in series. Similarly 0^ (4V6) in second circuit are in series[11, 12]. We may use backtracking if any problem is encountered.

0 →1 →4 →0 and

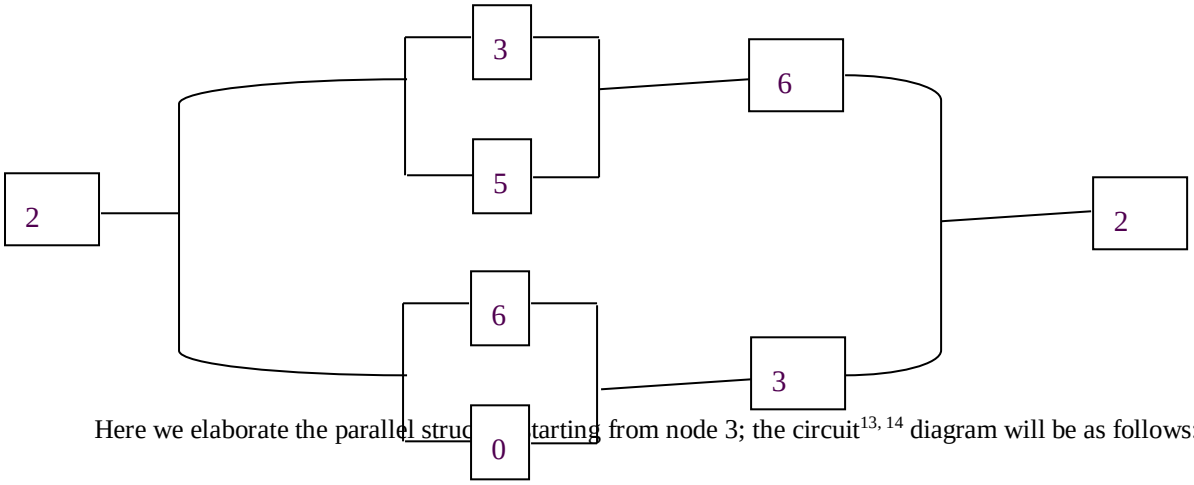
0 →3 →4 →0 are mixed structure, first stage is parallel but second stage is in series

Above structure is a specialized form of parallel programming for the purpose of sharing information between different nodes/devices. In contemporary systems, it is usually used for mediating between application and other node. Parallel structure allows programs to "hand off" work to be done by the node and then proceed to other tasks, or to not begin until input has been transcribed. A dedicated program, the flag, maintains an orderly sequence of instruction for the communication.

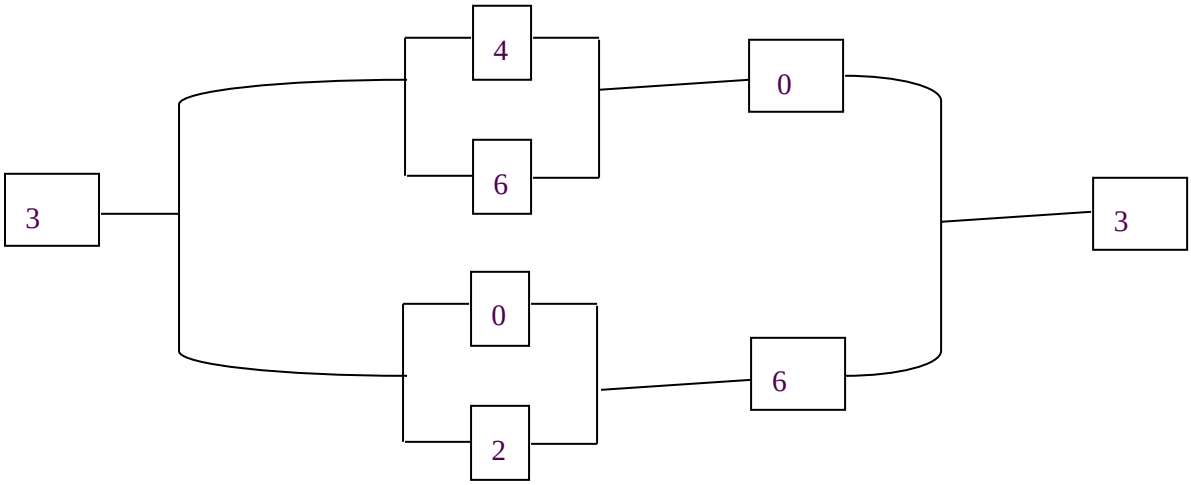
Here we elaborate the parallel structure starting from node 1; the circuit diagram will be as follows



Here we elaborate the parallel structure starting from node 2; The circuit diagram will be as follows:



Here we elaborate the parallel struc tarting from node 3; the circuit[13, 14] diagram will be as follows:



As we know the degree of each node is 4 in perfect difference network with d=2. Above circuit diagram of PDN explore at least two parallel structures[15, 16] in PDN. Initial and ending point show the common node it means all the above circuit is closed circuit. We may also change the final point if we need open circuit.

CONCLUSION

This paper presents PDN, a mature, frugal, flow-level topological properties for modelling large-scale networks and computing systems. PDN is designed to carry out performance-related studies of interconnection network for both HPC systems and datacentres. It features a completely modular design in which adding new topologies, routings or traffic models requires minimum effort. 0^ (1V3) and 0^ (4V6) both are in parallel but the next stage of communication is in series and the upcoming node is shared node with another parallel pattern. To avoid collision need some decision. This work gives some experience with parallel computing to know the potential and limitation of interconnection network. The purpose of this research work is to promote the understanding by focusing on topological properties and parallel structure that are naturally suited for high performance computing and that represent the best approach for solving communication problems.

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