



THE TASK ALLOCATION MODEL IN COMMUNICATION CHANNEL DELAY

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Abstract : In this paper a heuristics approach for task allocation in a distributed computing system has been discussed. This performs static allocation and provide near optimal results. The suggested algorithm is coded in Mat Lab and implemented on a Dual Core machine and found the performance of the developed algorithm is satisfactory.

Keywords: Distributed Computing System, mainframes, computational

1. INTRODUCTION

A Distributed Computing System (DCS) consists of any number of possible configurations, such as mainframes, personal computers, workstations, minicomputers, and so on. The goal of distributed computing is to the transparent data distribution within a local network. A user-oriented definition of distributed computing is "Multiple Computers, utilized cooperatively to solve problems" has been reported by {Sita [04], Chia [03], and Bhut [02]}. Distributed computing systems are of current interest for the researchers due to the advancement of microprocessor technology and computer networks {Till [05], Aror [01]}. In a DCS, the execution of a program may be distributed among several processing elements to reduce the overall cost of execution by taking advantage of inhomogeneous computational capabilities and other resources within the system. The task allocation in a DCS finds extensive applications in the faculties, where large amount of data is to be processed in relatively short period of time, or where real-time computations are required such as, Meteorology, Cryptography, Image Analysis, Signal Processing, Solar and Radar Surveillance, Simulation of VLSI circuits and Industrial process monitoring are areas of such applications.

2. PROBLEM STATEMENT

Consider a DCS consisting a set of n processors $P = \{p_1, p_2, \dots, p_n\}$, interconnected by communication links and a set of m tasks $T = \{t_1, t_2, \dots, t_m\}$ where $m > n$. An allocation of tasks to

Processors is defined by a function A_{alloc} from the set T of tasks to the set P of processors such that:

$A_{alloc}: T \rightarrow P$, where $A_{alloc}(i) = j$ if task t_i is assigned to processor p_j , $1 \leq i \leq m$, $1 \leq j \leq n$.

While designing the model it is assumed that Execution Cost (EC) of each task on all the Processors and the Data Transfer Rate (DTR) between the tasks is known and will be taken in the form Execution Cost Matrix [ECM (.)] of order $m \times n$, and Data Transfer Rate Matrix [DTRM(.)] of order m respectively. The communication channel delay is also considered and taken in the form of Channel Delay Matrix [CDM (.)] of order m .

3. PROPOSED METHOD

The allocation of tasks is to be carried out so that each task is assigned to a processor whose capabilities are most appropriate for the tasks, and their processing cost is to be minimized. The present model passes through the following phases.

Phase –I

Average Load:

The average load L_{avg} and Total Load (TL) is to be assigned on processor p_j with 05% Tolerance Factor (TF) has to be calculated as:

$$L_{avg}(p_j) = \frac{ec_{ij}}{m} \quad 1 < i < m, \quad 1 < j < n \dots \dots \dots 3.1$$

$$LT = \sum L_{avg}(p_j) + TF \dots \dots \dots 3.2$$

where $TF = \left(L_{avg}(p_j) \right) * \frac{0.5}{100}$ and $j = 1, 2, \dots, n$

Selection of “n” Task on the basis of minimum DTR:

The upper diagonal values of the DTRM (,) are stored in Maximum Data Transferred Rate Matrix MAXDTRM (,) of order $m(m - 1)/2$ by 3 the first column represents first task (say rth task), second column represent the second task (say sth task) and third column represent the DTR (drs) between these rth and sth tasks. The MAXDTRM (,) is then stored in ascending order assuming the third column as sorted key and select first tasks “n” which and store the tasks in $Ttasks(j)$ (where $j = 1,2, \dots, n$) and also store the remaining $m - n$ tasks in another linear array $TNtasks(k)$ (where $k = 1,2, \dots, m - n$).

Assignment: To get the initial assignment store the ECM (,) in NECM (,) $NECM (,) \leftarrow ECM (,)$ then reduce the $NECM(i,j)$ (where $i = 1,2, \dots, n$ and $j = 1,2, \dots, n$) in the square matrix of order n by deleting tasks stored in $TNtasks(k)$ which is the intersection of $Ttasks(i)$ and apply the YAS-Algorithm developed by Yadav et al [04]. The initial allocation is stored in an array $Tass(j)$ (where $j = 1,2, \dots, n$) and also the processor position are stored in a another linear array $Aalloc(j)$. Get the value of $TTASK(j)$ by adding the values of $Aalloc(j)$ if a task is assigned to a processor otherwise continue. Select a task from $TNtasks(k)$ (where $k = 1,2, \dots, m-n$) for assignment say tk and assign task to processor pj where the value of EC in minimum. Store the assignment and their position in $Tass(j)$ and $Aalloc(j)$ respectively and modify the $TTASK(j)$ by adding the value of $Aalloc(j)$. The $TNtasks(k)$ is also modify the by deleting the tasks tk . This process of assignment is continuing till the remaining “m-n” tasks are get allocated.

Phase -II

After completing the allocations the Processor’s Wise Execution Cost (PEC) ec_{ij} ($1 \leq i \leq m, 1 \leq j \leq n$) of each task ti on the processor pj is calculated using the following equation

$$PEC(A_{alloc})_j = \sum_{i \in TS_j, 1 \leq i \leq m} ec_i, A_{alloc}(j) \dots \dots \dots 3.3$$

where $TS_j = \{i: A_{alloc}(i) = j, j = 1,2, \dots, n$

Inter Processor Communication (IPC):

The Inter Processor Communication cost of the interacting tasks ti and tk is depends upon the per unit data transfer rate d_{ik} during the program execution is determined by using the equation given below Inter Processor Communication with delay (IPCWD) is calculated by the equation given below

$$IPCWD(A_{alloc})_j = [\min(ec_{ij} * d_{ij})] * cd_{ij},$$

$$j = 1,2, \dots, n \text{ and } i = 1,2 \dots, m \dots \dots \dots 3.4$$

Where cd_{ij} s the delay channel.

Inter Processor Communication without delay (IPCWOD) is calculated by the equation Given below

$$IPCWOD(A_{alloc})_j = [\min(ec_{ij} * d_{ij})] \quad j = 1,2, \dots, n \text{ and } i = 1,2 \dots, m \dots \dots \dots 3.4.1$$

Calculate the Overall Processors Cost [OPC] with delay and without delay calculated as

$$OPCWD(A_{alloc})_j = PEC(A_{alloc})_j + IPCWD(A_{alloc})_j \dots \dots \dots 3.5$$

$$OPCWD(A_{alloc})_j = PEC(A_{alloc})_j + IPCWOD(A_{alloc})_j \dots \dots \dots 3.5.1$$

and find the average Overall Processors Cost [OPC]

The Mean Service Rate [MSR] with delay and without delay of the processors are calculated by using the equation described below and store the results in MSR $(A_{alloc})_j$ (where $j = 1,2, \dots, n$).

$$MSRWD(A_{alloc})_j = \frac{1}{OPCWD(A_{alloc})_j} \quad \text{Where } j = 1,2, \dots, n \dots \dots \dots 3.6$$

$$MSRWD(A_{alloc})_j = \frac{1}{OPCWD(A_{alloc})_j} \quad \text{Where } j = 1,2, \dots, n \dots \dots \dots 3.6.1$$

The throughputs of the processors with delay and without delay are calculated by using the equation given below and store the results in a linear arrays $TRP(A_{alloc})_j$, where $j = 1,2 \dots, n$.

$$TRP(A_{alloc})_j = \frac{TTASK(A_{alloc})_j}{OPCWD(A_{alloc})_j} \text{ where } j = 1,2, \dots, n \dots \dots \dots 3.7$$

$$TRP(A_{alloc})_j = \frac{TTASK(A_{alloc})_j}{OPCWD(A_{alloc})_j} \text{ where } j = 1,2, \dots, n \dots \dots \dots 3.7.1$$

Finally, Critical Transmission Delay [CTD] and the Optimal Processing Cost (OPC) with delay and without delay have been determined. The maximum value of $OPC(A_{alloc})_j$ will be the Total System Cost (TSC) which shall be the optimal cost of the DCS.

3.4 ALGORITHM:

Step1: Input; m, n, ECM (.), DTRM (.) and CDM (.)

Step2: for i ← 1 to m do
for j ← 1 to n do

Determine the Total Load (TL) to be assigned on processor pj with 05% Tolerance Factor (TF) by using the equation (1) and (2) respectively.
repeat

repeat

Step3: k ← m(m - 1)/2

t ← m - n

for i ← 1 to m do
for j ← 1 to k do

Store the “k” upper diagonal value of DTRM (.) in MAXDTRM (.)
MAXDTRM (.) ← DTRM (.)

Arrange the MAXDTRM (.) ascending order
repeat

repeat

Step4: for i ← 1 to n do

for j ← 1 to n do

Store the ECM (.) in NECM (.)
NECM (.) ← ECM (.)

repeat

repeat

Step5: count ← n

for i ← 1 to m do

for j ← 1 to k do

Pick-up the minimum value from MAXDTRM (.) say tj, tk

If n = count;

Then

store the tasks in a linear array Ttasks() and go to the step-5

else;

Repeat for i

if MAXDTRM(i,j) < MAXDTRM(i,k)

bmin ← MAXDTRM(i,j) until j = k

bmin < MAXDTRM(i,k) until j = k

end if

check the corresponding position of bmin MAXDTRM(.) (say tl) and give one increment to count

count ← count + 1

store the tasks in a linear array Ttasks() also store the remaining m-n tasks in TNtasks()

repeat

repeat

Step 6: Reduce MAXDTRM (.) and also modify the NECM (.) by eliminating the tasks stored in Ttasks()

Step-7: Apply the YAS-Algorithm to get the initial allocation and store the assignment in an linear array

Tass(j) (where j = 1,2, ..., n) also the processor position are stored in a another linear array Aalloc(j). Get the

value of TTASK (j) by adding the values of Aalloc (j) if a task is assigned to a processor otherwise continue.

Step-7.1:

for i ← 1 to m do

store the TNtasks() in Tnon - ass()

Tnon - ass() ← TNtasks()

repeat

Step:7.2:

for i ← 1 to m - n do

for j ← 1 to n

Select a task from TNtasks (k) (where k = 1,2, ..., m - n) for assignment say ti and assign task to processor pj where the value of ecij is minimum.

Aalloc(k) ← j;

nomade ← nomade + 1;

Tass ← Tass ∪ {tk};

repeat

repeat

This process is continuing till the remaining “m - n” tasks are get allocated.

Step-8:

for $k \leftarrow 1$ to m do
 for $j \leftarrow 1$ to n do
 Compute the final $PEC(Aalloc)j$ using the equation (3.3)
 repeat
 repeat
Step-9:
 for $k \leftarrow 1$ to m do
 for $j \leftarrow 1$ to n do
 Compute the Inter Processor Communication Cost $IPC(Aalloc)j$ of the interacting tasks t_i and t_k by using the equation (3.4) and (3.4.1)
 repeat
 repeat
Step-10:
 for $i \leftarrow 1$ to m do
 Determine the finally, Overall Processors Cost $OPC(Aalloc)j$ by using the equation (3.5) and (3.5.1)
 repeat
Step-11:
 for $i \leftarrow 1$ to n do
 Compute the mean service rate $MSR(Aalloc)j$ by using the equation (3.6) and (3.6.1)
 repeat
Step-12:

for $i \leftarrow 1$ to n do
 Compute the processor's throughput by using the equation (3.7) and (3.7.1)
 Repeat
Step-13: Calculate the total Critical Transmission Delay [CTD] and the maximum value of $OPC(Aalloc)j$ i.e .the Total System Cost
Step-14:
 Stop.

3.5 IMPLEMENTATION OF THE ALGORITHM:

Example:
 To justify the application and usefulness of the present algorithm an example of a DCS is Considered which is consisting of $n = 3$ the set of processors $P = \{p1, p2, p3\}$ connected by an arbitrary network and $m = 6$ the set of tasks $T = \{t1, t2, t3, t4, t5, t6\}$ which may be portion of an executable code or a data file.

Step1:
 Input of the Algorithm: Data required by the algorithm is given below:
 Number of processors available in the system (n) = 3
 Number of tasks to be executed (m) = 8

	P1	P2	P3
t1	6	3	5
t2	4	2	3
t3	3	1	2
t4	5	2	∞
t5	3	4	2
t6	6	∞	6
t7	5	6	7
t8	∞	2	5

$$DTRM(.) = \begin{matrix} & \begin{matrix} t_1 & t_2 & t_3 & t_4 & t_5 & t_6 & t_7 & t_8 \end{matrix} \\ \begin{matrix} t_1 \\ t_2 \\ t_3 \\ t_4 \\ t_5 \\ t_6 \\ t_7 \\ t_8 \end{matrix} & \begin{pmatrix} 0.000 & 0.333 & 0.250 & 0.500 & 0.167 & 0.125 & 1.000 & 0.000 \\ 0.333 & 0.000 & 0.000 & 0.000 & 0.000 & 0.000 & 0.000 & 0.200 \\ 0.250 & 0.000 & 0.000 & 0.250 & 0.333 & 0.500 & 0.000 & 0.000 \\ 0.500 & 0.000 & 0.250 & 0.000 & 0.200 & 0.333 & 0.500 & 0.200 \\ 0.167 & 0.000 & 0.333 & 0.200 & 0.000 & 0.000 & 0.000 & 0.000 \\ 0.125 & 0.000 & 0.500 & 0.333 & 0.000 & 0.000 & 0.167 & 0.125 \\ 1.000 & 0.000 & 0.000 & 0.500 & 0.000 & 0.167 & 0.000 & 0.200 \\ 0.000 & 0.200 & 0.000 & 0.200 & 0.000 & 0.125 & 0.200 & 0.000 \end{pmatrix} \end{matrix}$$

$$CDM(.) = \begin{matrix} & \begin{matrix} t_1 & t_2 & t_3 & t_4 & t_5 & t_6 & t_7 & t_8 \end{matrix} \\ \begin{matrix} t_1 \\ t_2 \\ t_3 \\ t_4 \\ t_5 \\ t_6 \\ t_7 \\ t_8 \end{matrix} & \begin{pmatrix} 0 & 2 & 1 & 1 & 2 & 2 & 1 & 1 \\ 2 & 0 & 1 & 1 & 1 & 1 & 1 & 2 \\ 1 & 1 & 0 & 2 & 1 & 2 & 1 & 1 \\ 1 & 1 & 2 & 0 & 1 & 2 & 1 & 2 \\ 2 & 1 & 1 & 1 & 0 & 1 & 1 & 1 \\ 2 & 1 & 2 & 2 & 1 & 0 & 2 & 2 \\ 1 & 1 & 1 & 1 & 1 & 2 & 0 & 2 \\ 1 & 2 & 1 & 2 & 1 & 2 & 2 & 0 \end{pmatrix} \end{matrix}$$

Step2:After Implementation of the Algorithm’s steps the Average load to be assigned on the processors has been given in table 3.1

Table 3.1

Processors	Average execution cost
P1	5
P2	3
P3	4
Total Load	12
05% Tolerance Factor [TF]	0.6 (= 0.5 say)
Total Average load on the processor= Total load + TF]	12+0.5= 12.5

Step3:

The m (m-1)/2 i.e. 28 value of upper diagonal values of the DTRM (,) are stored in MAXDTRM (,):

$$\text{MAXDTRM} (.) = \begin{pmatrix} \text{t1} & \text{t2} & 0.333 \\ \text{t1} & \text{t3} & 0.250 \\ \text{t1} & \text{t4} & 0.500 \\ \text{t1} & \text{t5} & 0.167 \\ \text{t1} & \text{t6} & 0.125 \\ \text{t1} & \text{t7} & 1.000 \\ \text{t1} & \text{t8} & 0.000 \\ \text{t2} & \text{t3} & 0.000 \\ \text{t2} & \text{t4} & 0.000 \\ \text{t2} & \text{t5} & 0.000 \\ \text{t2} & \text{t6} & 0.000 \\ \text{t2} & \text{t7} & 0.000 \\ \text{t2} & \text{t8} & 0.200 \\ \text{t3} & \text{t4} & 0.250 \\ \text{t3} & \text{t5} & 0.333 \\ \text{t3} & \text{t6} & 0.500 \\ \text{t3} & \text{t7} & 0.000 \\ \text{t3} & \text{t8} & 0.000 \\ \text{t4} & \text{t5} & 0.200 \\ \text{t4} & \text{t6} & 0.333 \\ \text{t4} & \text{t7} & 0.500 \\ \text{t4} & \text{t8} & 0.200 \\ \text{t5} & \text{t6} & 0.000 \\ \text{t5} & \text{t7} & 0.000 \\ \text{t5} & \text{t8} & 0.000 \\ \text{t6} & \text{t7} & 0.176 \\ \text{t6} & \text{t8} & 0.125 \\ \text{t7} & \text{t8} & 0.200 \end{pmatrix}$$

The MAXDTRM (.) is stored in ascending order assuming the third column as sorted key and select those tasks “n = 3” which has minimum DTR and store the tasks in Ttasks(j) (where j =

1,2, ..., n) and also store the remaining m-n tasks in another linear array TNtasks(k) (where k =

1,2, ..., m - n).

$$\text{MAXDTRM} (,) = \begin{pmatrix} t1 & t8 & 0.000 \\ t2 & t3 & 0.000 \\ t2 & t4 & 0.000 \\ t2 & t5 & 0.000 \\ t2 & t6 & 0.000 \\ t2 & t7 & 0.000 \\ t3 & t7 & 0.000 \\ t3 & t8 & 0.000 \\ t5 & t6 & 0.000 \\ t5 & t7 & 0.000 \\ t5 & t8 & 0.000 \\ t1 & t6 & 0.125 \\ t6 & t8 & 0.125 \\ t1 & t5 & 0.167 \\ t6 & t7 & 0.176 \\ t2 & t8 & 0.200 \\ t4 & t5 & 0.200 \\ t4 & t8 & 0.200 \\ t7 & t8 & 0.200 \\ t1 & t3 & 0.250 \\ t3 & t4 & 0.250 \\ t1 & t2 & 0.333 \\ t3 & t5 & 0.333 \\ t4 & t6 & 0.333 \\ t1 & t4 & 0.500 \\ t3 & t6 & 0.500 \\ t4 & t7 & 0.500 \\ t1 & t7 & 1.000 \end{pmatrix}$$

Step4: Store the ECM (,) in NECM,) as:

$$\text{NECM}(,) = \begin{matrix} & \begin{matrix} p1 & p2 & p3 \end{matrix} \\ \begin{matrix} t1 \\ t2 \\ t3 \\ t4 \\ t5 \\ t6 \\ t7 \\ t8 \end{matrix} & \begin{pmatrix} 6 & 3 & 5 \\ 4 & 2 & 3 \\ 3 & 1 & 2 \\ 5 & 2 & \infty \\ 3 & 4 & 2 \\ 6 & \infty & 6 \\ 5 & 6 & 7 \\ \infty & 2 & 5 \end{pmatrix} \end{matrix}$$

$$\leftarrow \text{ECM}(,) = \begin{matrix} & \begin{matrix} p1 & p2 & p3 \end{matrix} \\ \begin{matrix} t1 \\ t2 \\ t3 \\ t4 \\ t5 \\ t6 \\ t7 \\ t8 \end{matrix} & \begin{pmatrix} 6 & 3 & 5 \\ 4 & 2 & 3 \\ 3 & 1 & 2 \\ 5 & 2 & \infty \\ 3 & 4 & 2 \\ 6 & \infty & 6 \\ 5 & 6 & 7 \\ \infty & 2 & 5 \end{pmatrix} \end{matrix}$$

Step5:

$Ttasks() = \{ t1\ t8\ t5 \}$

$TNtasks() = \{ t2\ t3\ t4\ t6\ t7 \}$

Step6:

Reduced NECM(.) and MXDTRM(.)

$$NECM(.) = \begin{matrix} & \begin{matrix} p1 & p2 & p3 \end{matrix} \\ \begin{matrix} t1 \\ t5 \\ t8 \end{matrix} & \begin{pmatrix} 6 & 3 & 5 \\ 3 & 4 & 2 \\ \infty & 2 & 5 \end{pmatrix} \end{matrix}$$

$$MAXDTRM (.) = \begin{pmatrix} t2\ t3\ 0.000 \\ t2\ t4\ 0.000 \\ t2\ t5\ 0.000 \\ t2\ t6\ 0.000 \\ t2\ t7\ 0.000 \\ t3\ t7\ 0.000 \\ t3\ t8\ 0.000 \\ t5\ t6\ 0.000 \\ t5\ t7\ 0.000 \\ t1\ t6\ 0.125 \\ t6\ t8\ 0.125 \\ t1\ t5\ 0.167 \\ t6\ t7\ 0.176 \\ t2\ t8\ 0.200 \\ t4\ t5\ 0.200 \\ t4\ t8\ 0.200 \\ t7\ t8\ 0.200 \\ t1\ t3\ 0.250 \\ t3\ t4\ 0.250 \\ t1\ t2\ 0.333 \\ t3\ t5\ 0.333 \\ t4\ t6\ 0.333 \\ t1\ t4\ 0.500 \\ t3\ t6\ 0.500 \\ t4\ t7\ 0.500 \\ t1\ t7\ 1.000 \end{pmatrix}$$

Step7:

Initial assignments are obtained by applying the YAS-Algorithm developed by Yadav et al [Yada04] are given in Table 3.2:

Table 3.2 Initial Assignment

Tasks	Processor	EC
t5	p1	3
t8	p3	5
t1	p2	3

Step7.1:

$Tnon - ass () \leftarrow TNtasks ()$

$Tnon - ass () = \{ t2\ t3\ t4\ t6\ t7 \}$

$Aalloc (j) = \{ 1, 3, 2 \}$ and $TTASK (j) = \{ 1, 1, 1 \}$

After Implementing the Step-7.2 the following final assignment are obtained.

Table 3.3: Final Assignment

Tasks	Processor	EC
t3 + t5 + t7	p1	11
t1 + t2 + t4	p2	07
t6+ t8	p3	11

The final $Aalloc(j) = \{ 1, 3, 2, 1, 1, 2, 2, 3, 3 \}$ and $TTASK (j) = \{ 3, 3, 2 \}$, Table 3.3 shows the final assignment after Implementation of assignment procedure described in section 3.3 in the proposed method. On applying the further steps 8 to 13 following result are obtained and shown in the table 3.4

Table – 3.4:

Processors	EC	IPC without Delay	IPC with Delay	OPC without Delay	OPC with Delay	MSR without Delay	MSR with Delay	TRP without Delay	TRP with Delay	Total critical Transmission Delay
1	2	3	4	5=2+3	6= 2+4	7	8	9	10	11=6-5
P1	11.000	5.079	7.658	16.079	18.658	0.062	0.054	0.124	0.107	2.579
P2	7.000	4.882	7.364	10.882	13.364	0.092	0.075	0.276	0.224	2.482
P3	11.000	3.705	6.510	13.705	16.510	0.073	0.061	0.219	0.182	2.805

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