



Harmonic Mitigation Using DC Self Supported Shunt Active Power Filter

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Abstract: The advent of semiconductor technology has resulted in increased application of power electronic devices in industrial as well as domestic loads, a combination of which acts as a non-linear load. These non-linear loads are responsible for increased harmonics by drawing a distorted current from the supply system, leading to deterioration of source currents and voltages. This work proposes a method to improve the power quality with the aid of a three-phase shunt active power filter (SAPF) implementing a controlled voltage source inverter and synchronous d-q reference current generation technique for reference current generation of hysteresis controller. A discrete PI controller has been implemented to maintain a constant DC capacitor link voltage. The proportional and integral gains of the PI controller have been computed with the help of bacterial foraging optimization technique. The proposed SAPF for a three phase three wire system employing a balanced non-linear load has been simulated on MATLAB software to validate its performance. The simulation results demonstrate satisfactory performance of the proposed SAPF by effectively compensating harmonics of the supply system and lowering THD such that they fall within IEEE 519 standards for harmonic levels.

Keywords: harmonic compensation; hysteresis current controller; shunt active power filter (SAPF); synchronous reference frame (SRF) theory

I. INTRODUCTION

Intensive use of power electronic equipment has led to increased harmonics in supply system. These harmonics deteriorate the power quality by distorting the current and voltage waveforms hence pose a major drawback issue in the power transmission network. Harmonics in supply system apart from damaging the source have also caused increased losses in transmission lines, power cables, transformers and end devices connected to the power system. Hence it is necessary to eliminate these harmonics in order to reduce power losses and safeguard our system from damages.

Initially passive filters were used to filter out the harmonic current and remove harmonic distortion but these filters suffer from drawbacks such as resonance with source, bulky in size and fixed compensation. Also, these passive filters can be designed to filter out harmonics of known frequencies only and not those harmonics whose frequencies are unknown to us. Hence active power filters came into application since they mitigate harmonics of all orders from the supply. The shunt active power filter (SAPF) absorbs harmonics by injecting a harmonic compensating current and reactive power requirement of the load at the point of common coupling (PCC).[1]

This paper puts forward a design for shunt active power filter (SAPF) based on synchronous reference frame current theory (SRF method). Hysteresis current controller is implemented to generate gate pulses of the three-phase voltage source inverter and the DC link voltage of the inverter is maintained constant by a PI controller whose gains are tuned by bacterial foraging optimization technique. Simulation model of the shunt active power filter implemented for the harmonic mitigation of a rectifier controlled non-linear load is designed in MATLAB software. Simulation results depict that harmonic

distortion has reduced and lies well within limits specified by IEEE 519 standards.

II. SHUNT ACTIVE POWER FILTER (SAPF)

In this the active power filter is connected in parallel with the source to mitigate the harmonic current of the load as well as inject reactive power at the PCC thereby improving the power factor of the supply. It also reduces losses due to harmonics resulting in increased efficiency.[2]

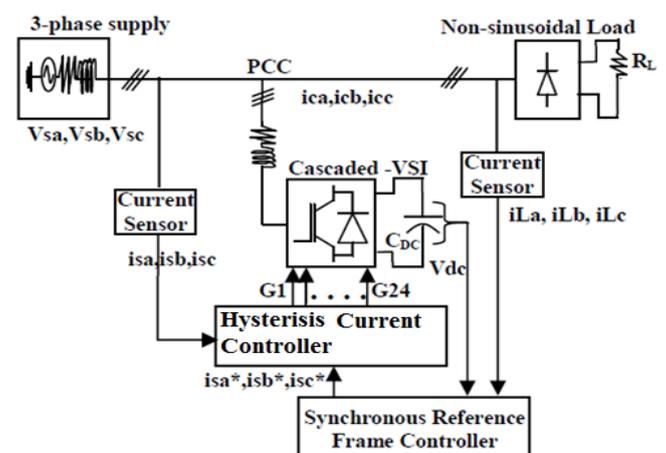


Fig 1 shunt active power filter

A. Basic Working Principle

SAPF operates to generate a compensating current equal to the harmonic current drawn by the non-linear load but opposite in phase. As a result harmonics are not passed onto supply side due to which supply current consists of only fundamental current component i.e. free from harmonics.

The SAPF consists of a reference current generator, a hysteresis current controller, voltage source inverter, DC link capacitor and a coupling inductor. The load side harmonics are detected and reference current generated by SRF method. This reference current is compared with the actual filter current in hysteresis current controller to generate gate pulses for the voltage source inverter (VSI). The inverter generates compensating currents which is fed to the main supply system at PCC with the help of a coupling inductor acting as a current limiter.

III. SYNCHRONOUS REFERENCE FRAME (SRF) THEORY

SRF method is implemented to extract the harmonic content from the load current by transforming three phase source currents (I_{sa}, I_{sb}, I_{sc}) to instantaneous active (I_d) and reactive components (I_q) with the aid of Park Transformation. Park Transformation is a method of transforming three phase time varying currents into two phase reference frame rotating synchronously with the positive sequence component of the system voltage. In the synchronously rotating reference frame, the components at fundamental frequency, are transformed to dc quantities and all harmonic components undergo a frequency shift of ω₁ (=50Hz). The Park transformation matrix is given as follows:

$$\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\omega t & \cos(\omega t - 120) & \cos(\omega t + 120) \\ \sin\omega t & \sin(\omega t - 120) & \sin(\omega t + 120) \\ 0.5 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}$$

Eq (1)

Where ‘ωt’ is the speed of the rotating d-q frame of reference i.e. the phase of the positive sequence source voltages. The functions sin ωt and cos ωt are derived from the phase locked loop (PLL) circuit which performs the work of synchronizing the system with fundamental frequency of source voltage. The direct and quadrature axis currents are composed of both the ac and dc components.[3,4]

$$I_d = I_d^{dc} + I_d^{ac} \tag{Eq (2)}$$

$$I_q = I_q^{dc} + I_q^{ac} \tag{Eq (3)}$$

The DC component is filtered out with the help of a low pass filter (LPF) from I_{sd} and I_{sq}. the extracted DC components (I_{sdDC}, I_{sqDC}) are again transformed into a-b-c coordinate. this transformation is called as inverse parks transformation.

$$\begin{bmatrix} I_{sa*} \\ I_{sb*} \\ I_{sc*} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\omega t & -\sin(\omega t) & 1 \\ \cos(\omega t - 120) & -\sin(\omega t - 120) & 1 \\ \cos(\omega t + 120) & -\sin(\omega t + 120) & 1 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix}$$

Eq (4)

A. Reference current generation

Reference current will be generated with the help of PLL and Parks transformation and then compared with the actual line current. Output of which is given into the hysteresis controller.

I_{sa*}, I_{sb*} and I_{sc*} are the reference current generated, as shown in Fig (2).

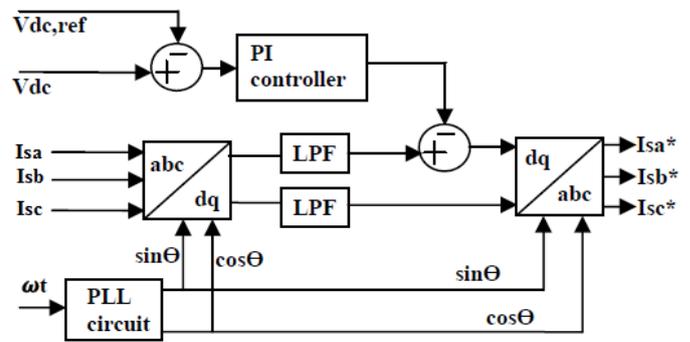


Fig 2 Reference current generation

IV. HYSTERESIS CURRENT CONTROLLER

The performance of inverter and its nature is controlled by the control unit. A hysteresis current controller is used in this paper for controlling the output of inverter. Controlling strategy of hysteresis current controller is based on an error signal between a reference current (I_{ref}) and actual current (I_{actual}). This error signal generates control signals for inverter switches by hysteresis comparators.[6,7]

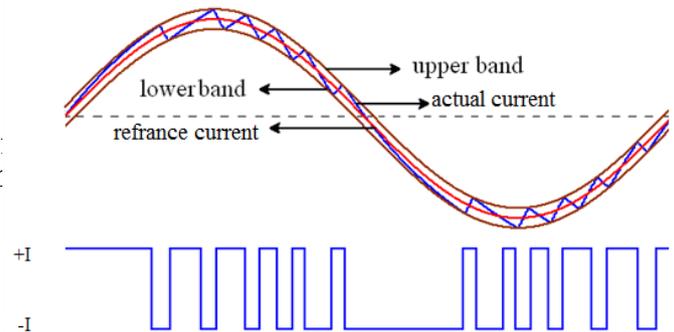


Fig 3 Hysteresis band

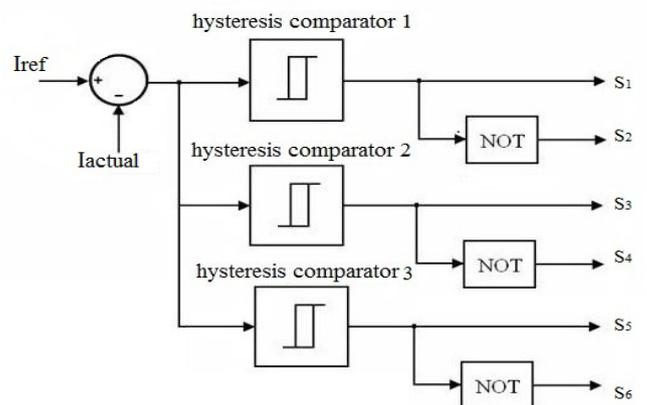


Fig 4 Switching of devices with hysteresis controller

Shunt active power filter is comprised of 3-phase IGBTs based voltage source inverter (VSI) bridge to allow independent current control. Switching of the upper device and lower device in one phase leg of VSI are complementary.[5]

On the above and below of reference current two bands are present called as upper hysteresis band (UHB) and lower hysteresis band (LHB). When the difference of reference current and actual current is reaches to UHB/LHB, current forced to decrease/increase.

V. SIMULATION RESULTS

Simulink model of system with non linear(rectifier) load is shown in Fig(5).

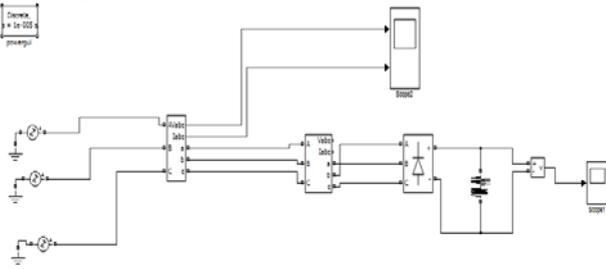


Fig 5 Simulink model of system without SHPF
Voltage and current waveform of source is shown in fig(6) without implementation of SHPF with non linear load.

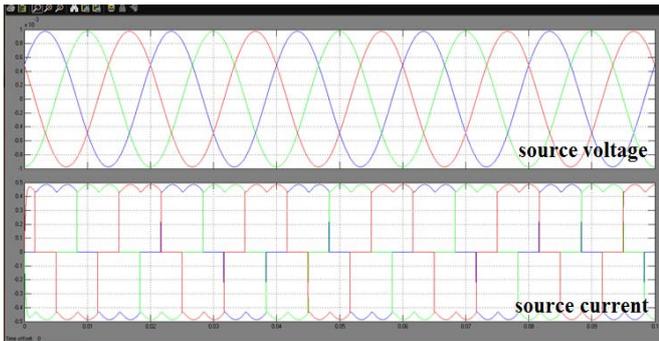


Fig 6 Source voltage and current waveform without SHPF

Without implementation of shunt active power filter THD of source current is calculated and shown in fig (7). Calculated THD is 30.79%.

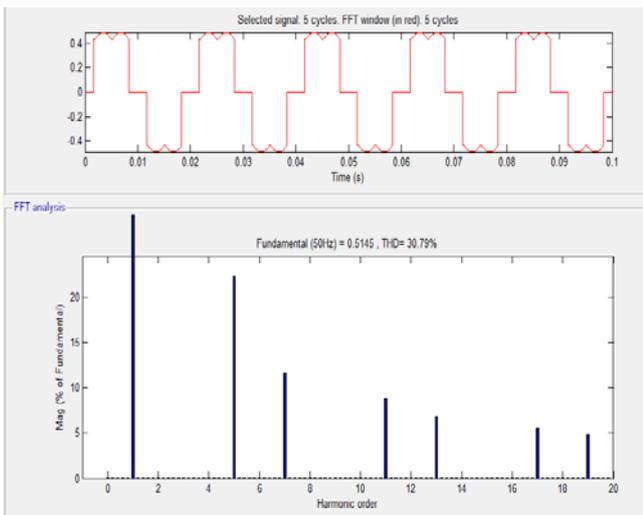


Fig 7 THD of source current without SHPF

Now shunt active power filter is employed in same system, shown in fig (8) and THD of source voltage is calculated, as shown in fig(9).

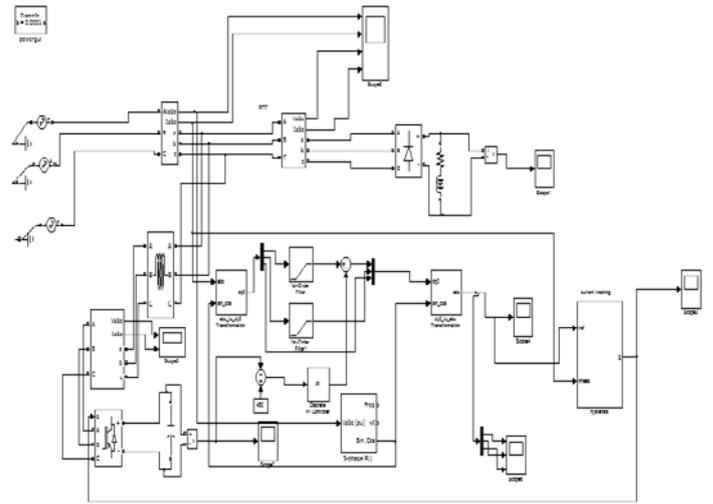


Fig 8 Simulink model of system with SHPF

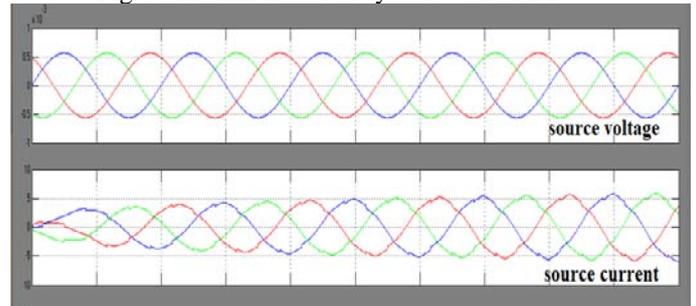


Fig 9 Source voltage and current waveform with SHPF

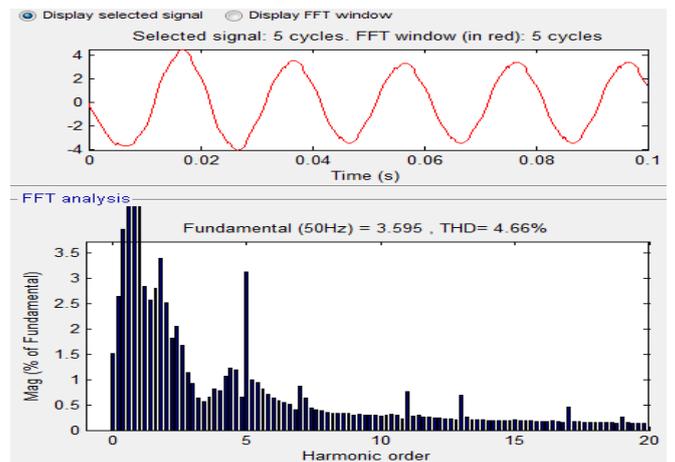


Fig9 THD of source current with SHPF

The Fast Fourier Transform (FFT) is used to measure the order of harmonics with the fundamental frequency at 50 Hz for the source current. The total harmonic distortion (THD) measured at the source current on the distribution system and various harmonic order measured without APF and with APF are presented in Table 1.

Table 1

Significant Harmonic	THD Magnitude (%)	
	Without APF	With APF
5 th	22.28	3.14
7 th	11.70	0.88
11 th	8.85	0.75
13 th	6.79	0.68

15 th	0.06	0.22
17 th	5.54	0.45
THD	30.79	4.66

APPENDIX

PARAMETERS	VALUES
Input voltage	230 V
Input frequency	50 Hz
L_f	2mH
C_{dc}	1200 μ F
Switching frequency	600Hz
K_p	0.2
K_i	1
R	5ohm
L	1mh
V_{dcref}	450

VI. CONCLUSION

In this paper, an inverter based shunt active power filter for medium voltage applications has been simulated. Harmonics are detected through the SRF and the reference current has been generated and switching PWM pulses are obtained from hysteresis current controller. Shunt APF is found injecting compensating current, thereby reduces the magnitude of the significant harmonics in the line current and hence the THD. It can be seen from simulation results that THD level is considerably reduced (from 30.79 % to 4.66 %), and comes under the limit specified in IEEE 519.

VII. REFERENCES

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