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RF mixer design for 10.5 GHz, using 0.18µm CMOS technology

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Abstract **-**This paper present area efficient design for 10.5 GHz RF mixer using 0.18µm CMOS technology. VLSI Technology includes process design, trends, chip fabrication, real circuit parameters, circuit design, electrical characteristics, configuration building blocks, switching circuitry, translation onto silicon, CAD, practical experience in layout design. The proposed mixer is designed using 0.18µm CMOS/VLSI technology, which can be used in front end of a superheterodyne receiver. Simulations were performed using the Agilent advance designing software, TSMC model. Results indicate that mixer provides gain of 13.69dB at a noise figure of 10.29dB. Finally the mixer layout is designed using Microwind designing software within area 0.6mm^2.

Keywords: Gilbert mixer cell, LNA, LO, 0.18µm, VLSI technology, low power.

I. INTRODUCTION

Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems. It is widely felt today that ICs in advanced bipolar & GaAs technologies will provide the best solutions in terms of the sought performance at the lower power dissipation. For operation at RF in the GHz band CMOS is a viable alternative.

The mixer in the receiver posses an even a greater design challenge because the intermediation distortion between an interference signal passing through the preselection filter & the desired signal may produce in-band spurious signals, & irrecoverably degrade the received signal to noise ratio. Signals received from the antenna are passed to a band pass filter before being fed into the LNA. The LNA amplifies the incoming signal which is then supplied to the mixer that performs the frequency conversion. The design of the mixer can be distinguished in three major sections, a wide band radio frequency (RF) front-end mixer (250MHz), an image-rejection (IR) mixer and intermediate frequency (IF) stage. The front-end of the mixer consists of a low noise amplifier (LNA), a low pass filter (LPF) & a high linearity mixer.

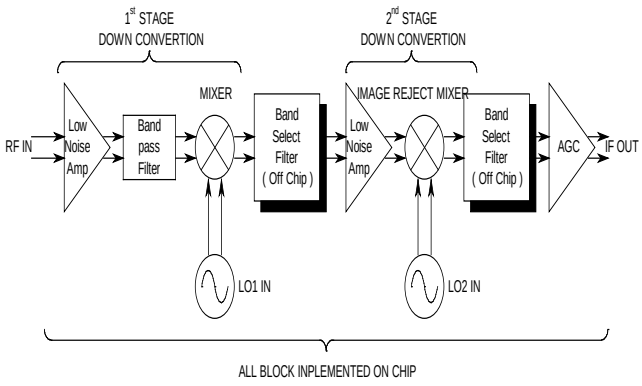


Figure. 1 Integrated Mixer block diagram

The RF mixer specifications that have to be met in this design are shown in table I. It is desired to have sufficient gain with low noise. It is important to optimize the metrics of noise figure & gain for the system because a low noise figure is desired for injecting less noise into the system. Finally the design should provide the required amount of gain with sufficient linearity.

TABLE I: DESIRED CHARACTERISTICS AND SPECIFICATION OF MIXER SYSTEM

Features	Specification
Voltage Conversion Gain	≥10dB
1 dB Compression Point	≥- 5.6dBm
Input Referred IP3	≥5.6dBm
Single Sideband Noise Figure	≤10dB
IF Frequency	250MHz
RF Frequency	10.5GHz
LO Frequency	10.25GHz
Supply Voltage	≤ 1.8V
Power consumption	≤ 39mW
Operating Current	≤ 15mA
Area	0.6mm^2
Process	0.18µm CMOS

II. CONVENTIONAL GILBERT CELL

Linear time invariant (LTI) system produces output that oscillates at the same frequency as the inputs. Hence to generate an output signal at different frequency from the input a non linear element is necessarily required. At the heart of all mixer design is the fundamental identity

$$(A\cos\omega_1 t)(B\cos\omega_2 t)=\frac{AB}{2}[\cos(\omega_1-\omega_2)t+\cos(\omega_1+\omega_2)t]----(1)$$

Where ω_1 & ω_2 corresponds to the RF and the LO frequencies which generates the IF output at the difference of the two frequencies. Note that the amplitude of the output is directly proportional to the amplitude of the RF signal

provided the amplitude of the local oscillator is kept constant.

CMOS implementations generally use the square law behavior of long- channel devices to generate the produced term in eq. (1) where the sum of the RF and the LO signal is used as the gate voltage to generate the IF term at the output. Simple circuits that try to implement this idea lead to very poor LO-IF isolation. Hence mixers that directly multiply the two signals are generally found to have much better performance characteristics.

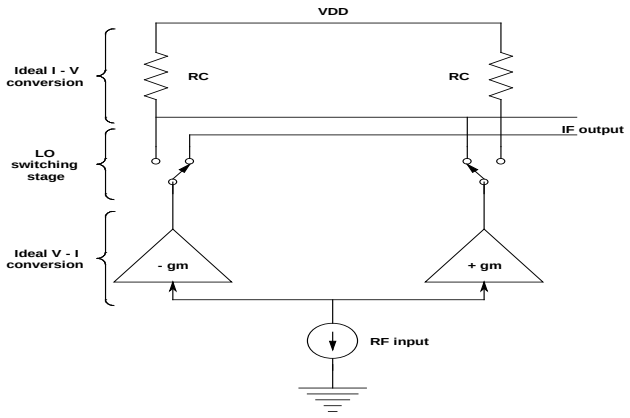


Figure. 2 illustrating diagram of Gilbert mixer cell

In the design of Mixer there are several conflicting goals, these includes minimizing the noise figure providing high gain with sufficient linearity. With these goals in mind Gilbert mixer architecture was chosen initially.

The most common of mixer topologies is the double balanced configuration known as the Gilbert Cell. This design is often chosen over the simpler single balanced configuration due to it's LO feed through isolation properties. Double balanced mixers use symmetry to cancel unwanted LO components while enhancing desired mixing components at the output. Refer to Figure 2 for an illustrated diagram of a double balanced mixer. The basis of mixing relies on the multiplication of two signals, the LO signal and an incoming information signal, the RF signal. The voltage of the RF signal is amplified and converted into a current by a driver stage. The LO signal is used to steer all of the current from one transistor to the other at the LO switching stage. Finally, the IF output voltage is created due to the current through the load resistors.

Figure 3 shows the schematic of the Gilbert cell type double balance mixer which is obtained by combining two single balanced mixers, such as local oscillator terms are added. Thus the mixer provides the better LO-IF isolation as compared to a single balanced mixer.

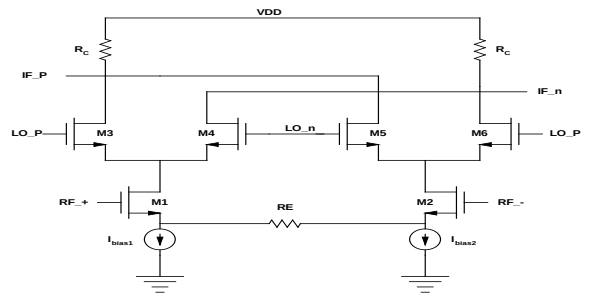


Figure. 3 Schematic of Gilbert mixer.

The gain of the LNA exacerbates any nonlinearity in the mixer and serves to reduce the impact of noise generated within the mixer. Hence it is imperative to maintain the good linearity in the mixer at the cost of gain & noise. The conversion gain of the mixer is directly proportional to the transconductance of the RF transistor & is a straight forward tradd-off to obtain better linearity. Reducing the transconductance also leads to a reduction of the total noise figure of the mixer. The non ideal switching of the LO transistor also leads to noise and hence a high drive at the LO terminal helps to reduce the noise. It is also needed to note that any excess overdrive on the LO input leads to increase in non-linearity to the capacitive loading of the common source connection. To improve the linearity of the design the emitter of the RF transistor was inductively degenerated, which has the well-known advantage of low noise and no DC voltage headroom, as compared to a resistive degeneration.

III. PROPOSED MIXER ARCHITECTURE

The double balanced Gilbert Cell was chosen to initiate the design process. Upon initial simulation results of the Gilbert cell configuration, it was apparent that the specified design goals would not be achievable. The specified gain for the mixer was to be at least 10dB, however following several optimization attempts; the maximum achieved gain was approximately 5dB. It became necessary to choose a different circuit configuration, which allow for achieving higher gain. A mixer topology, which proclaims to allow for higher gain is known as a "Folded" Mixer As such, the remainder of this paper will be dedicated to "Current Folded RF Mixer design", architecture and strategies.

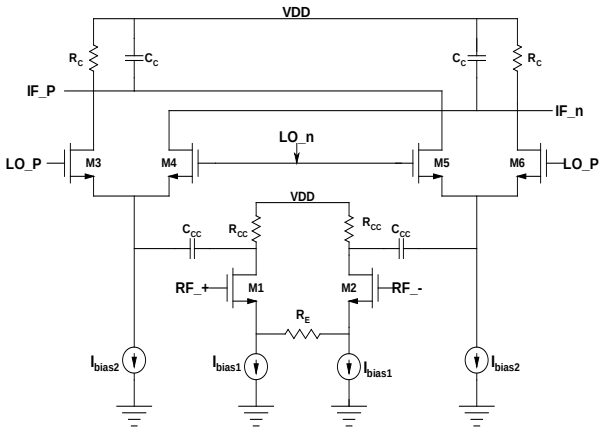


Figure.4 Proposed Mixer Architecture.

The most noticeable physical differences in conventional Gilbert mixer topology and folded mixer topology can be illustrated by Figure 4; here we see that the driver stage transistors (transconductance stage) are removed from the switching quad. The structure of the driver stage transistors now closely resembles that of a simple differential pair amplifier. Input RF current is amplified and fed into the switching quad network as in conventional Gilbert mixers. Ensuring that only AC current will flow into the switching quad, coupling capacitors C_{cc} are used, the size of these capacitors will be limited by process restrictions and chip area. Driver stage load resistors R_{cc} are implemented such that input RF current will flow up

into the switching quad with sufficient gain and that transistors M_1 and M_2 are properly biased. Degeneration resistor R_E will provide the overall mixer with improved linearity and stability during temperature fluctuations. The switching quad comprises of NMOS transistors M_3, M_4, M_5 and M_6, these transistors will oscillate (between on and off states) according to the input frequency of the LO. Load resistors R_C are used to convert mixed signal current into output IF voltage, the size of these resistors will influence the overall gain of the system and will be limited by remaining headroom voltage. Capacitors C_c will be implemented so that the output signal will be tuned to the output frequency, (the IF frequency). Both RF and LO input signals and the IF output signal are fully differential.

The attractiveness of the Folded Mixer design is attributed to the strong improvement in mixer gain. As devices M_3, M_1 and the current sink device require a certain voltage drop across them such that they are able to function in the saturation region of operation, any remaining voltage (supply voltage less mixer operation voltage) can be applied across the load resistor R_C. Mixer operation Voltage is the voltage required to keep Driver, Switching and Current Sink transistors in saturation. In the case of the Folded Mixer design, the mixer operation voltage is decreased by approximately 1.5V, this is because the driver stage is now separate from the switching quad and current sink transistors. This serves to alleviate headroom restrictions in that a larger voltage can now be applied across the load resistors R_C. By simply investigating Ohm's law V= I*R and noting that current remains fixed, it is apparent that an increase in voltage drop across resistor R_C will serve to increase the size of resistor R_C. Since the gain of the mixer is closely related to the output resistance, Rc, a larger load resistor will imply a higher gain.

IV. PROPOSED MIXER DESIGN

The design procedure of the mixer is basically comprised of executing several simulations until a desired result or mixer performance was achieved. There are several factors, which reflect mixer performance, such as gain, linearity, power and noise performance.

Adjusting circuitry for the purpose of optimizing a particular performance parameter may serve to unintentionally degrade the performance of the other parameter. It is important to monitor all of the performance parameters throughout the design process. The first stage in the design process was to approximate values for each circuit element in the mixer. The following discussion will outline how these approximations were achieved for transistor.

A. Transistor Operation

All transistors are needed to operate in the saturation region. For this requirement to be met, two expressions must be satisfied,

$$V_{GS} \geq V_{TH}$$
$$V_{DS} \geq V_{GS} - V_{TH}$$

Once these conditions have been satisfied it is possible to approximate the transistor behavior in the saturation region through the following equation,

$$I_D = \tfrac{1}{2}\, \mu_n C_{ox} W/L\, (V_{GS} - V_{TH})^2$$

The parameters which remain fixed in the above equation are μ_n, C_{ox}, L and V_{TH}. The parameters which can be adjusted for optimization are I_D, W and V_{GS}.

B. Transistor biasing

A common practice in RFIC design is to ensure that the gate bias voltage relative to the source voltage V_{GS} is between 200mV and 400mV above the threshold voltage V_{TH}.

$$V_{GS} - V_{TH} \geq V_{safety}$$

Where:

$$200mV \leq V_{safety} \leq 400mV$$

Further stage of the design process is to properly bias the mixer such that each transistor component will function in the correct region of operation. Beginning from the lowest voltage in the ckt. We note that the current sink requires a minimum of approximately 0.4 V for efficient operation. So current sink is designed at the s/w level & its simulation result is observed.

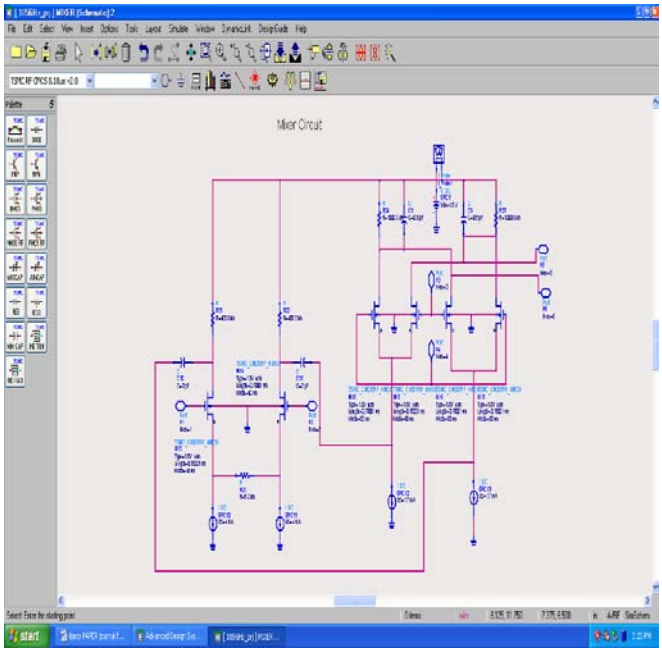


Figure.5 Simulated circuit of Current Folded mixer.

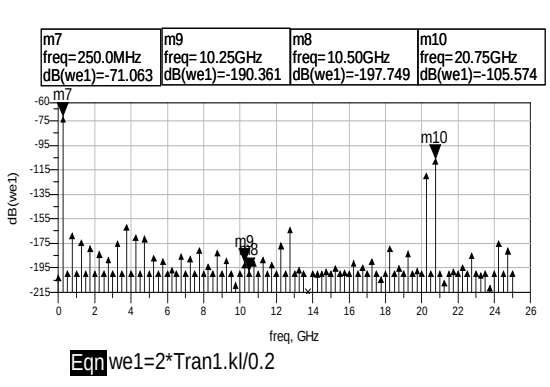
V. SIMULATION RESULTS

In this section, we discuss the results obtained from simulations and compare them with the required specifications. All simulations were performed using Agilent advanced designing s/w TSMC model & finally mixer layout was designed using Microwind.

A. Mixer Performance

[a] Voltage Conversion Gain

The mixer should provide sufficient voltage gain with low noise figure. Simulation 1 gives the spectra of o/p IF, the voltage conversion gain obtained is 13.69 dB.



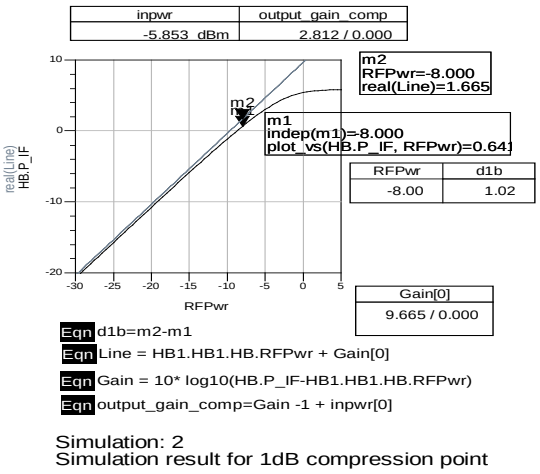


Figure.7 (a) Simulation for linearity.

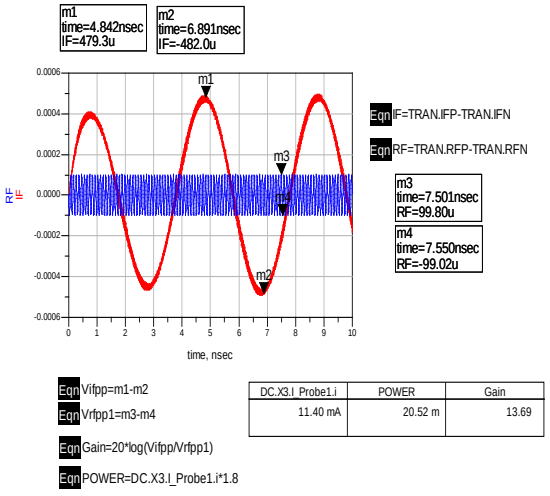


Figure.6 Voltage conversion gain.

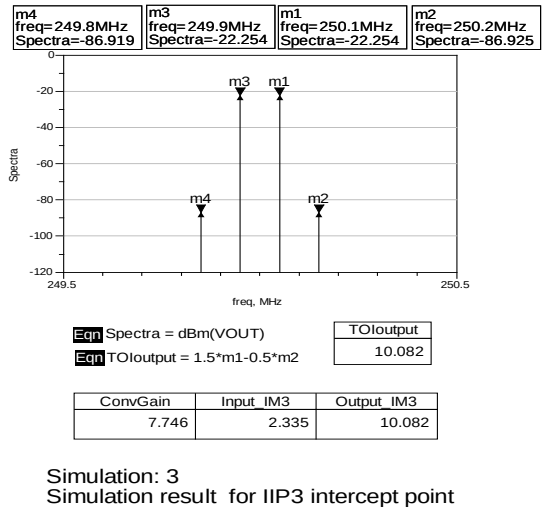


Figure.7 (b) Simulation for linearity.

[b] 1 dB Compression Point.

The 1dB compression point is the point where the output power is 1dB less than that of the ideal gain for a given input power. In order to determine the 1dB compression point of the mixer, a swept periodic steady state response (SPSS) analysis is used. In SPSS analysis RF input power, is swept from -30dB to 0dB as shown in figure 7(a). Simulation result shows that the 1dB compression point or P1dB occurs when the mixer receives an input of -8 dBm.

[c] IIP3 Intercept point

The SPSS analysis is used in conjunction with a periodic AC analysis to determine the third order intermodulation point. These simulations are combined and used to analyze two small signal input tones at the RF input. These tones occur at the expected input frequency of 2.51GHz and at an interfering signal (a neighboring channel frequency) of 2.52GHz.

[d] Single side band Noise Figure

The single sideband noise figure of the mixer was found by using the SPSS analysis followed by a Periodic Noise analysis. The Pnoise analysis computes the total noise contribution to the input signal from the circuit. Noise is contributed to the mixer from components such as resistors and transistors, input and output sources and frequency translation. Simulation results show that single sideband noise figure is 10.29dB.

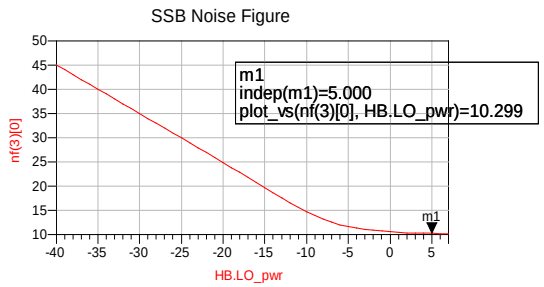


Figure.8 Simulation 4: SSB noise Figure.

TABLE II: RF MIXER PERFORMANCE SUMMARY

Performance measure	Mixer Specification	Simulation Result	Deduction
Conversion Gain	≥ 10dB	13.69dB	Pass
1 dB Compression Point	≥ - 5.6dBm	-8dBm	Acceptable
Input Referred IP3	≥ 5.6dBm	2.33dBm	Acceptable
SSB Noise Figure	≤ 10dB	10.29dB	Pass
IF Frequency	250MHz	250MHz	Pass
RF Frequency	10.5GHz	10.5GHz	Pass
LO Frequency	10.25GHz	10.25GHz	Pass
Supply Voltage	≤ 1.8V	1.8V	Pass
Power consumption	≤ 39mW	20.52mW	Pass
Operating Current	≤ 15mA	11.4mA	Pass

VI. CONCLUSION

A high gain, low voltage, low power current folded down conversion mixer is presented. This mixer is designed & implemented in 0.18µm CMOS technology. The main advantages of the proposed mixer topology are high RF range (10.5GHz), high voltage gain (13.69 dB), moderate noise figure (10.29dB), moderate linearity (IIP3 = 2.23dBm), operation at low supply voltage (V_{dd} = 1.8V) as listed in table II. Proposed layout of RF mixer consumes a very low power supply (39mWatt) and occupies a small chip area (0.6mm^2) compared to the previous mixers. Fig.9 depicts the mixer layout.

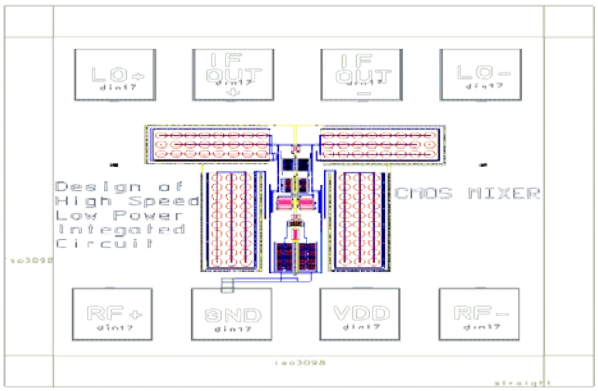


Figure.9 mixer layout

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