Volume 1, No. 2, July-August 2010

ISSN No. 0976-5697

International Journal of Advanced Research in Computer Science

REVIEW ARTICLE

Available Online at www.ijarcs.info

A Review of an Area Efficient Interpolation Filter and Computationally Efficient Interpolation filter Architecture for Digital Audio Applications

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Abstract: The paper describes a detailed review of area efficient architecture of interpolation filter for digital audio application. In this paper high speed and computationally efficient architecture of interpolation filter is also discussed. In this paper, work done by different researchers on efficient interpolation filter architectures is reviewed and a comparison is done on the basis of this review

Keywords: Merged Delay Transformation, Area Efficient Architecture, Interpolation Filter, Recursive Filter.

I. INTRODUCTION

Nowadays digital audio resources are used almost everywhere. Its increasing utility has drawn the attention of the researchers. So the work started on its efficient implementation architectures. In digital audio D/ A converters, Interpolation is required. Work has been done on a various types of interpolation filter architectures. Most common types of them are cascaded integrator comb (CIC) filters, polyphase filter structures and frequency response masking (FRM) approach. Most of the work is on FIR based interpolation filters because of their linear phase response. But on the other side their complexity increases rapidly. For such applications, IIR filters are a better option as compared to FIR filter [1]. IIR filters are more efficient and flexible than FIR filters. In addition to these advantages of IIR filters, their use was limited in past because of their non linearity and instability. In order to overcome these shortcomings the researchers have proposed the architecture of recursive filters by the name of Merged Delay Transformation [3, 4] for the implementation of both area efficient and computationally efficient filter architectures.

Section II gives the details of area efficient interpolation filter architecture [1]. Section III gives the details of high speed and computationally efficient filter architecture [2]. Section IV gives the comparison of both the architectures. Section V concludes the paper.

II. AREA EFFICIENT INTERPOLATION FILTER STRUCTURE

Merged Delay Transformed Interpolators

Figure 1 and 2 are showing the first and second order interpolation filters based on merged delay transformation.

Modified merged delay transformed interpolators

It can be observed from the interpolation filters in fig 1 and fig 2 that a large silicon area is required for their implementation and it is proportional to their L factor. For area efficiency the authors have replaced the 'L' multipliers by a single multiplier and a shift register which is operating at output clock. After this modification the filter structures for both the first order and second order filters are shown in figure 3 and figure 4.

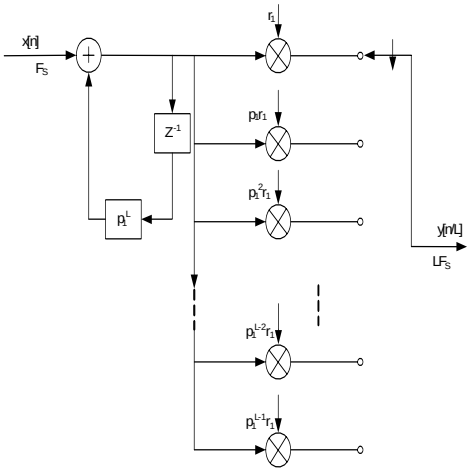


Figure 1. First order Merged Delay Transformed Interpolation filter [1].

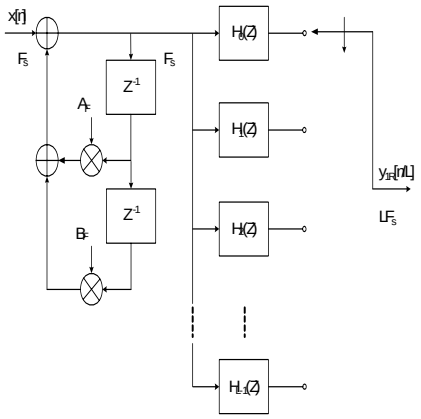


Figure 2. Second order Merged Delay Transformed Interpolation filter [1].

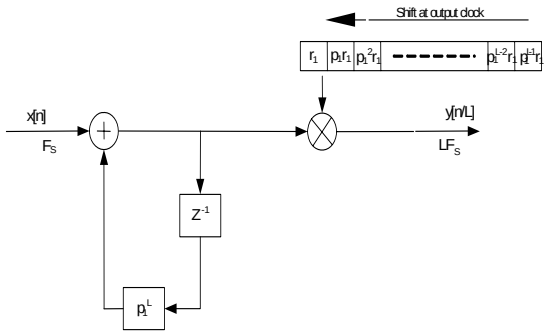


Figure 3. Modified Efficient Architecture for first order MDT Interpolator [1].

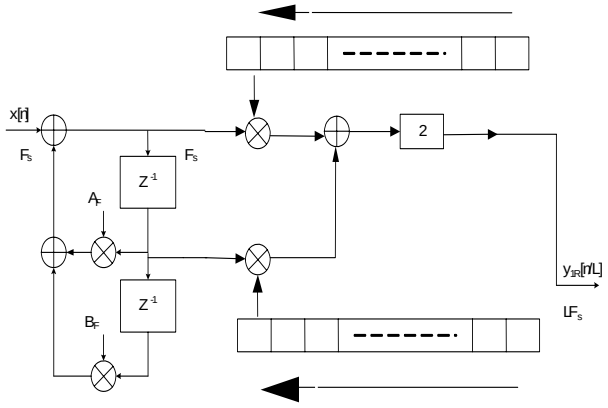


Figure 4. Modified Efficient Architecture for second order MDT Interpolation filter [1].

Figure 3 and Figure 4 show the hardware efficient architectures in which the number of multipliers is reduced occupying small silicon area. But the disadvantage of this structure is that if multipliers operate in a slow fashion it will make the entire interpolation slow, so we need high speed multipliers. But it does not affect audio applications badly because for audio applications the interpolation factor is not so high.

The silicon area covered by the proposed architecture is computed in the units of "Equivalent Gate Count". The result for modified MDT filter is shown in fig.5. It is also compared with the other three architectures and found to be more area efficient as compared to the existing filters [1].

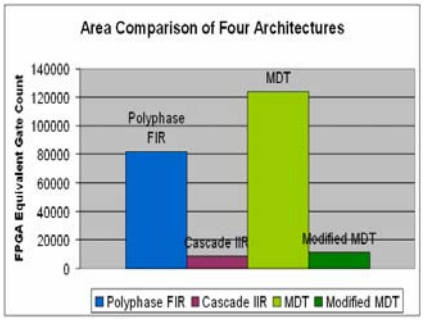


Figure 5. Comparison of Area in terms of FPGA equivalent gate count for four architectures based on synthesis results [1].

III. HIGH SPEED COMPUTATIONALLY EFFICIENT INTERPOLATION FILTER STRUCTURE

In this paper, [2] the researchers introduced a new architecture of computationally efficient and high speed recursive interpolation filter. The design of stable IIR filters is started using the existing filter design techniques. Any higher order IIR filter is divided into parallel first order sections. In order to transform the first order recursive filter into an interpolation filter merged delay transformation is used. Similarly for second order filter a pair of first order filter sections was used [2]. In the transformed architecture the filter runs on the input clock speed which makes the filter efficient in terms of power consumption. It is found that the proposed architecture has small critical path delay and it is stable. Also to check the computational costs authors compared the proposed architecture with different conventional filters and the proposed architecture is found to be more efficient. The proposed efficient interpolation filter structures are shown in figure 6 and 7.

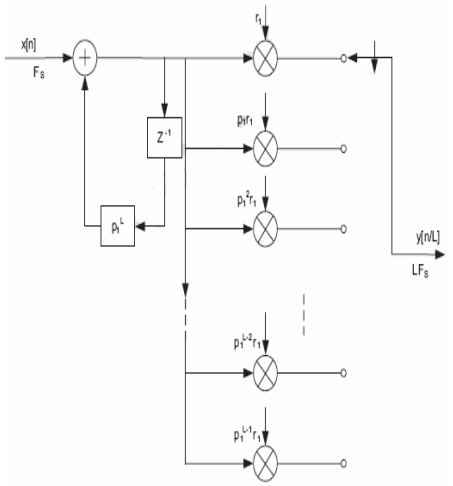


Figure 6. Architecture for first order filter transformed in to 1 to L interpolation filter [2]

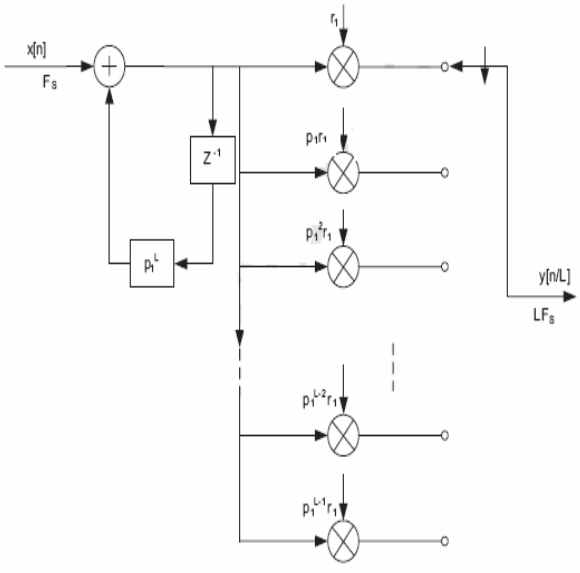
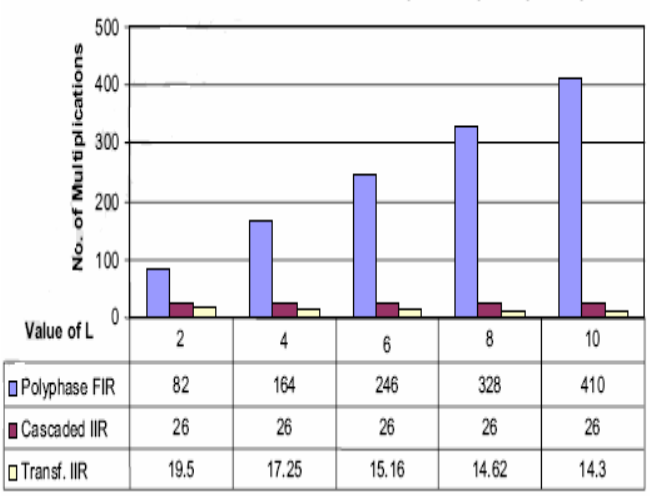


Figure 7. Architecture of second order IIR filter transformed into interpolation filter [2].

IV. RESULTS

Figure 8 shows the computational costs of the transformed filters, compared with the known architectures. It is observed from the graph that reduced computational cost of 89.48% was achieved as compared to polyphase FIR filter and it is 33.65% as compared to cascaded IIR interpolation filter [2].



Value of L	2	4	6	8	10
Polyphase FIR	82	164	246	328	410
Cascaded IIR	26	26	26	26	26
Transf. IIR	19.5	17.25	15.16	14.62	14.3

Figure 8. Comparison of computational costs of different architectures [2].

V. COMPARISON

On the basis of this review if we compare both the architectures of interpolation filter then we come to know that area efficient filter occupies small silicon area but due to the introduction of serial input register and slow multiplier operation, it is computationally slow. On the other hand computationally efficient interpolation filter is faster in performing computations but in terms of area it occupies more silicon area as compared to the previous proposed design. So more work can be done on the architecture of area efficient filter so that some other resource can be introduced in order to provide input to filter in parallel without affecting the area occupied by the filter and also by the use of faster multipliers its speed can be enhanced.

VI CONCLUSION

Implementation and results of area efficient interpolation filter proposed and implemented by the researchers is discussed in the paper. The architecture and results of computationally efficient interpolation filter is discussed. Finally both the architectures are compared.

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