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Comparative Study and Analysis of Universal Gates for Minimizing Power and Delay using Lector Technique

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Abstract: The main objective of this paper is to provide new low power solutions for Very Large Scale Integration (VLSI) designers The power consumption of the electronic devices can be reduced by adopting different design styles. Lector logic style is said to be an attractive solution for such low power electronic applications. The proposed technique has less power dissipation when compared to the conventional CMOS design style. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level. In this paper, Conventional NAND gate and Nor gate are designed and then compared with the Lector NAND and NOR using 180nm technology.

Keywords: Power dissipation, delay, transistors, leakage power, Lector, CMOS.

I. INTRODUCTION

As technology shrinks, power consumption and delay becomes an essential parameter. From mobile phone to laptops, every electronics gadgets is designed to have minimum power consumption and delay. Power consumption plays an important role in the present day VLSI technology [1]. Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost. If an IC is consuming more power, then a better cooling mechanism would be required to keep the circuit in normal conditions. Otherwise, its performance is degraded and on continuous use it may be permanently damaged [2].

II. OVERVIEW OF POWER DISSIPATION

It is more convenient to talk about power dissipation of digital circuits at this point. Although power depends greatly on the circuit style, it can be divided, in general, into static and dynamic power. The static power is generated due to the DC bias current, as is the case in transistor-transistor-logic (TTL), emitter-coupled logic (ECL), and N-type MOS (NMOS) logic families, or due to leakage currents. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. That is the reason why CMOS is the most suitable circuit style for very large scale integration (VLSI)[3].

The power consumption in conventional CMOS circuit is due to switching activity of the devices from one state to another state and due to the charging and discharging of load capacitor at the output node. The power dissipation in conventional CMOS design can be minimized by reducing the supply voltage, node capacitance value and switching activity [4]. But reducing the values of these parameters may degrade the performance of the device. So an efficient low power technique other than CMOS is needed that has less power dissipation compared to CMOS which can be done by using Lector technique.

III. LECTOR TECHNIQUE FOR POWER REDUCTION

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated that “a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path”. The number of OFF transistors is related to leakage power as shown in Figure 1.

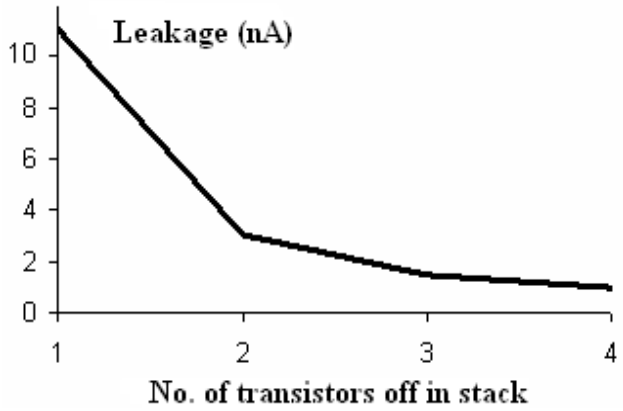

Figure 1. Transistor-stacking Vs Leakage Power.

In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage

control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cut off region[5].

This technique is implemented to universal gates such as NAND and NOR[6] .

IV. PROPOSED WORK

Logic gates are fundamental building blocks of digital integrated circuits. Logic gate is idealized or physical device implementing a boolean function i.e, it performs a logical operation on one or more inputs and produces a single logical output. There are seven basic logic gates:
NOT, AND, OR, NAND, NOR, XOR, XNOR[3].

A. NAND Gate:

Operation When A=0 and B=0, both the nMOS transistors are OFF and both pMOS are ON. Hence, the output is connected to V_{DD} and we get logic high at the output .When A=1 and B=0, the upper nMOS is ON and lower nMOS is OFF, so the output cannot be connected to the ground. Under this condition left pMOS is OFF but right pMOS is ON. Hence, the output is connected to V_{DD} we get logic high at the output. When A=0 and B=1, the upper nMOS is OFF and lower nMOS is ON, so the output cannot be connected to the ground. Under this condition left pMOS is ON but right pMOS is OFF. Hence, the output is connected to V_{DD} we get logic high at the output. When A=1 and B=1, both the nMOS transistors are ON and both the pMOS transistors are OFF. Hence the output is connected to the ground and we get logic low at the output[4].

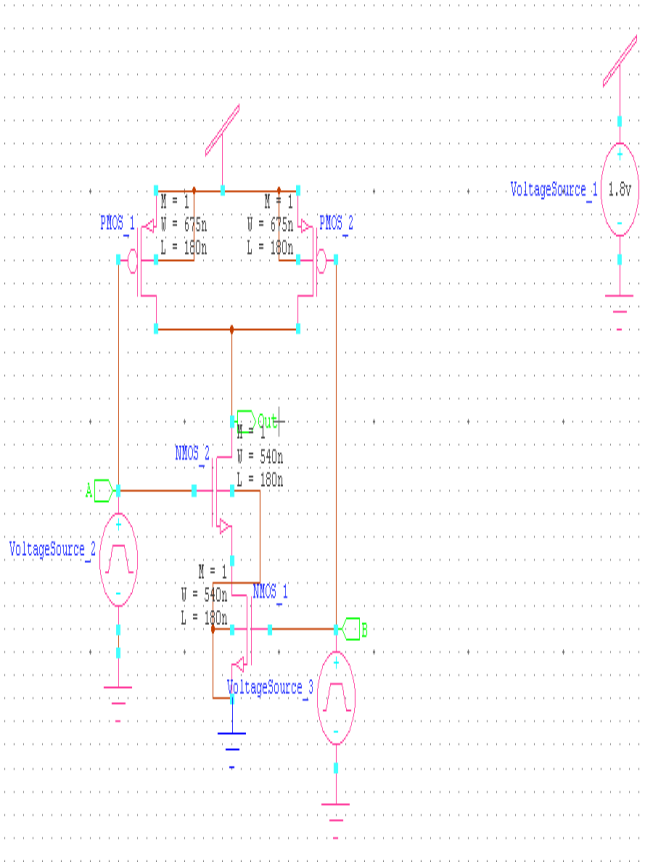

Figure 2 Conventional CMOS NAND Gate

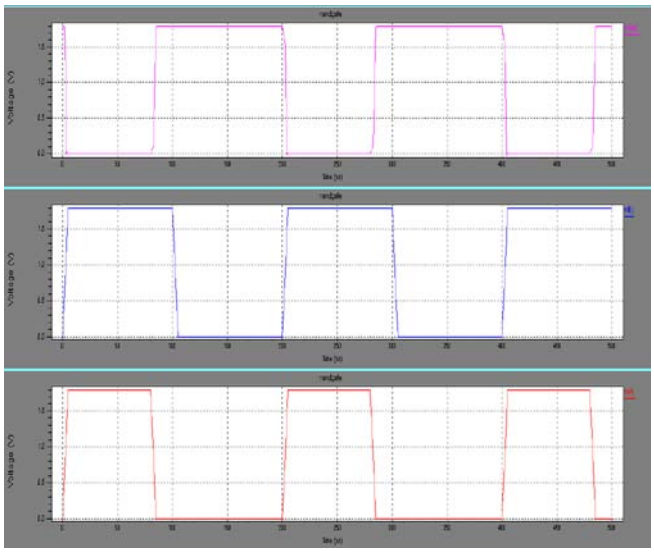

Figure 3 Waveform for Voltage of Conventional NAND gate

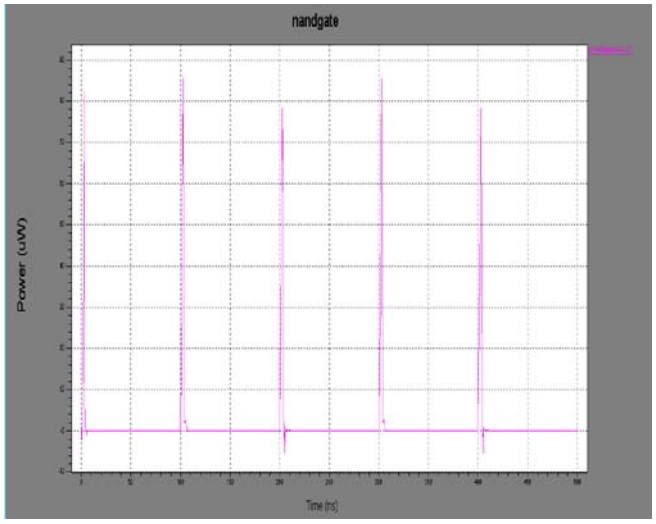

Figure 4 Waveform for power of Conventional NAND gate

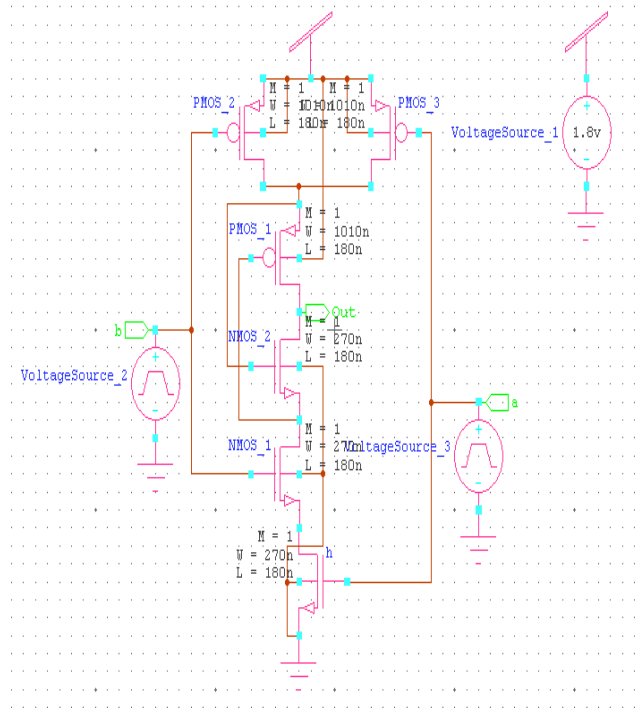

Figure 5 Circuit for NAND gate using lector technique

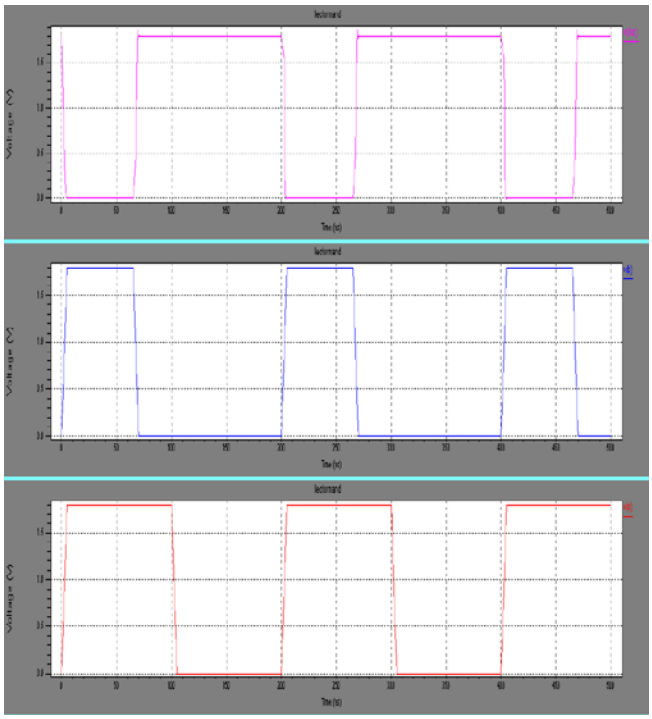

Figure 6 Waveform for NAND gate Voltage using Lector technique

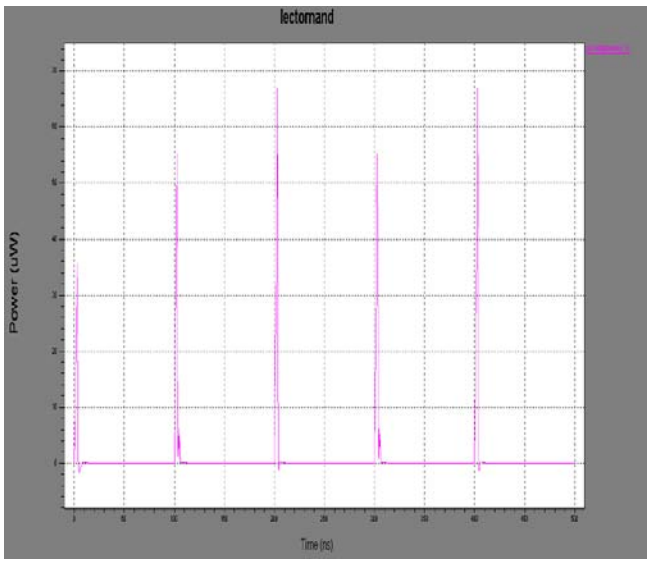

Figure 7 Waveform for NAND gate Power using Lector technique

B. NOR Gate:

Operation When A=0 and B=0, both the nMOS transistors are OFF and both pMOS transistors are ON. Hence, the output is connected to V_{DD} and we get logic high at the output.

When A=1 and B=0, the upper pMOS is ON and lower pMOS is OFF, so the output cannot be connected to the V_{DD} . Under this condition left nMOS is ON but right nMOS is OFF. Hence, the output is connected to ground we get logic low at the output.

When A=0 and B=1, the upper pMOS is ON and lower pMOS is OFF, so the output cannot be connected to the V_{DD}. Under this condition left nMOS is OFF but right nMOS is ON. Hence, the output is connected to ground we get logic low at the output.

When A=1 and B=1, both the nMOS transistors are ON and both the pMOS transistors are OFF. Hence the output is connected to the V_{DD} and we get logic low at the output[4].

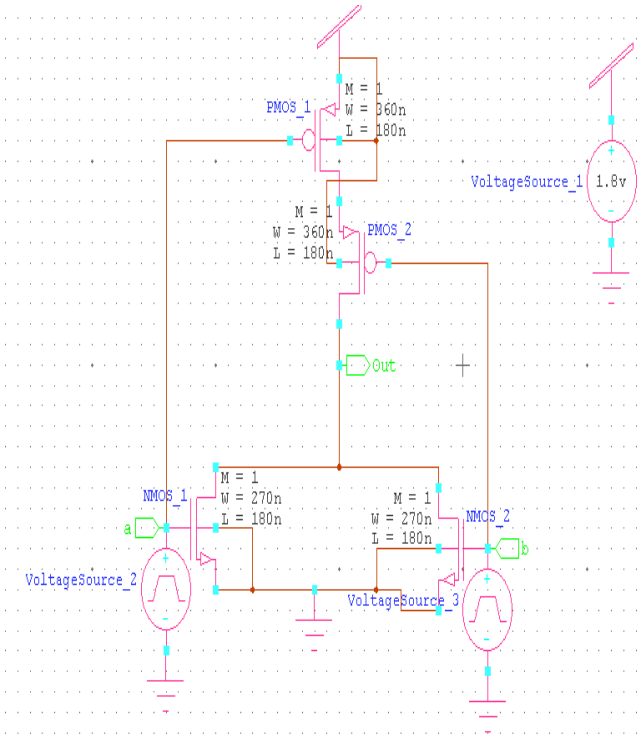

Figure 8 A Conventional CMOS NOR Gate

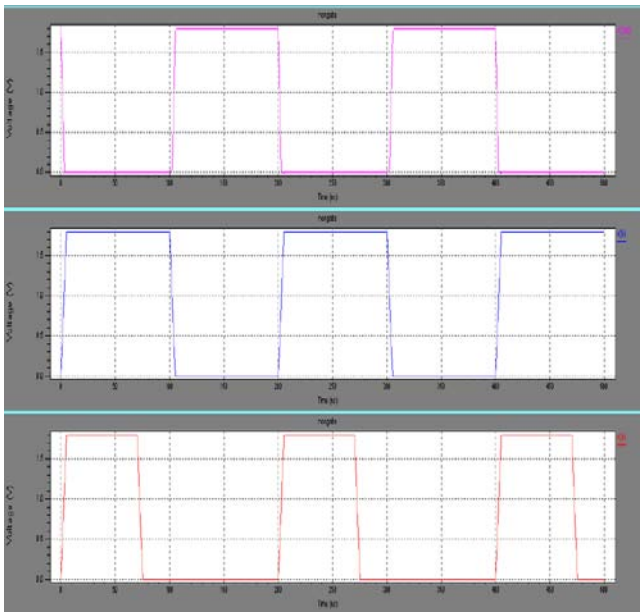

Figure 9 Waveform for Conventional NOR gate Voltage

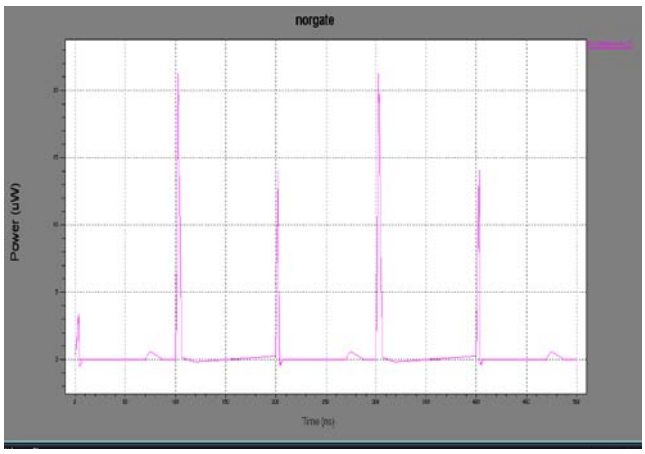

Figure 10 Waveform for Conventional NOR gate Power

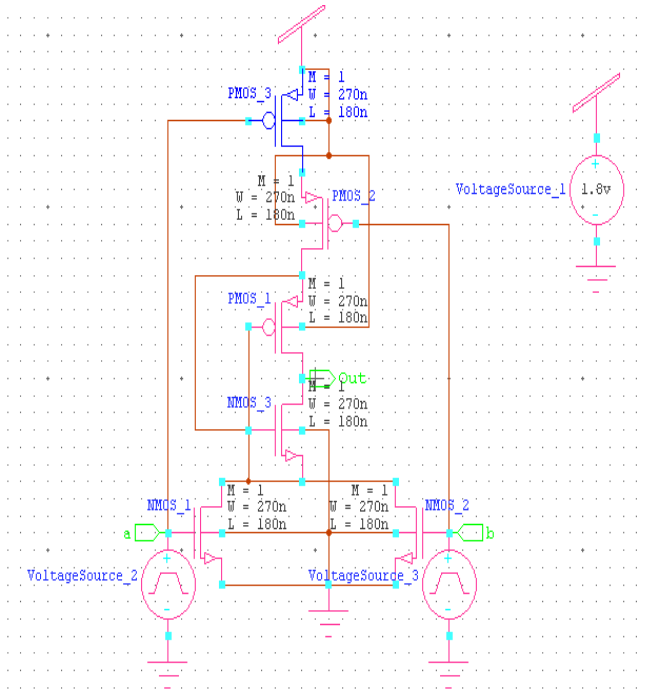

Figure 11 Circuit for NOR gate using lector technique

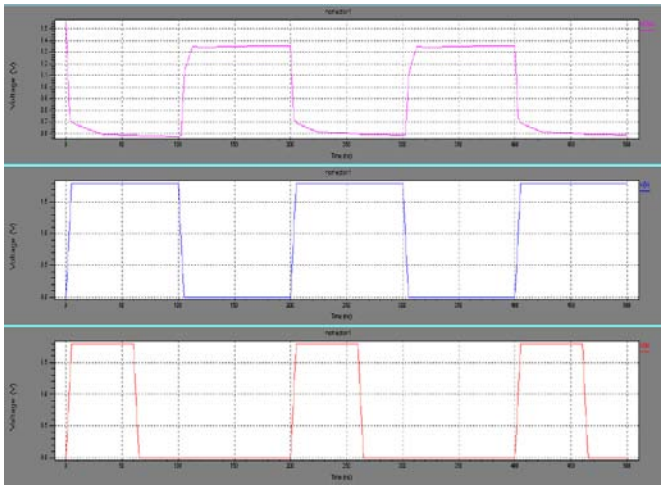

Figure 12 Waveform for Lector NOR gate voltage

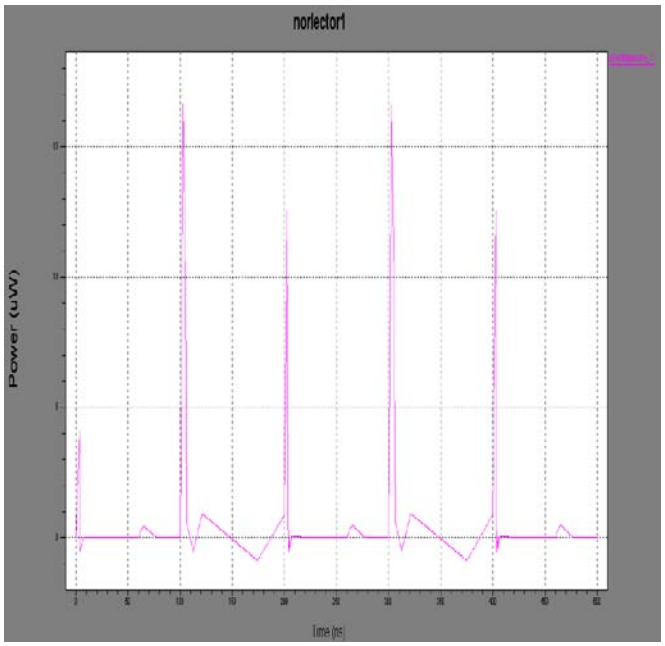

Figure 13 Waveform for Lector NOR gate Power

V. RESULTS

The proposed technique in the thesis is "LECTOR" and proposed technique is more effective in reducing power consumption[7].

The Simulation of logic gates with and without low power techniques is carried out at 180nm, technology. CMOS technology parameters are taken for NMOS and PMOS transistors, using TSPICE tool. Transient Analysis is done to get Delay and Average Power results .We have studied Lector power reduction technique compare this power reduction technique with CONVENTIONAL CMOS design

In this section result table showing Average Delay and Average Power Dissipation for Conventional and Lector logic gates is shown.

Table 1 Average Delay And Average Power Dissipation Results For Nand Gate

POWER REDUCTION TECHNIQUES	**AVERAGE DELAY** (In Nanoseconds)	**AVERAGE POWER DISSIPATION** (In Microwatts)
Conventional	0.36071	1.438965
Lector	0.85591	1.003443

Table 2 Average Delay And Average Power Dissipation Results For Nor Gate

POWER REDUCTION TECHNIQUES	**AVERAGE DELAY** (In Nanoseconds)	AVERAGE POWER DISSIPATION (IN MICROWATTS)
Conventional	0.17084	0.3150228
Lector	0.85384	0.278182

VI. CONCLUSION

Comparison Graphs for Power dissipation and Delay has shown in fig 14 and fig 15[8] :

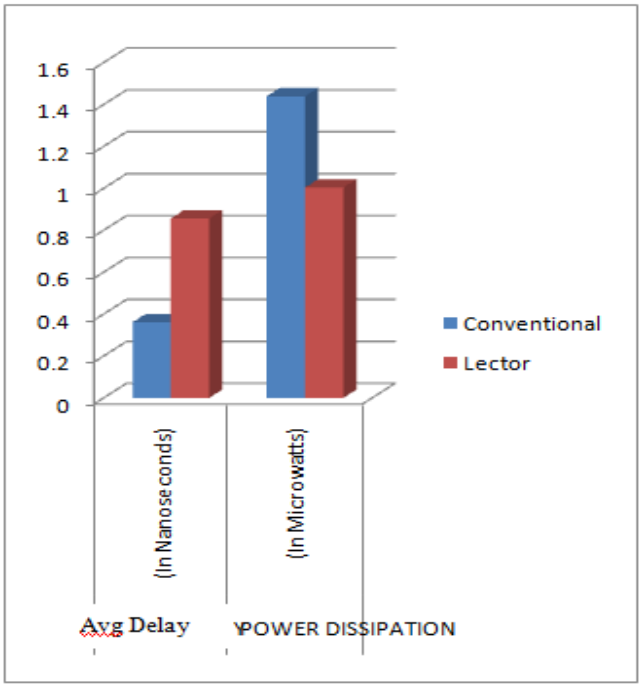

Figure 14 Comparison of Average Delay and average Power for NAND Gate

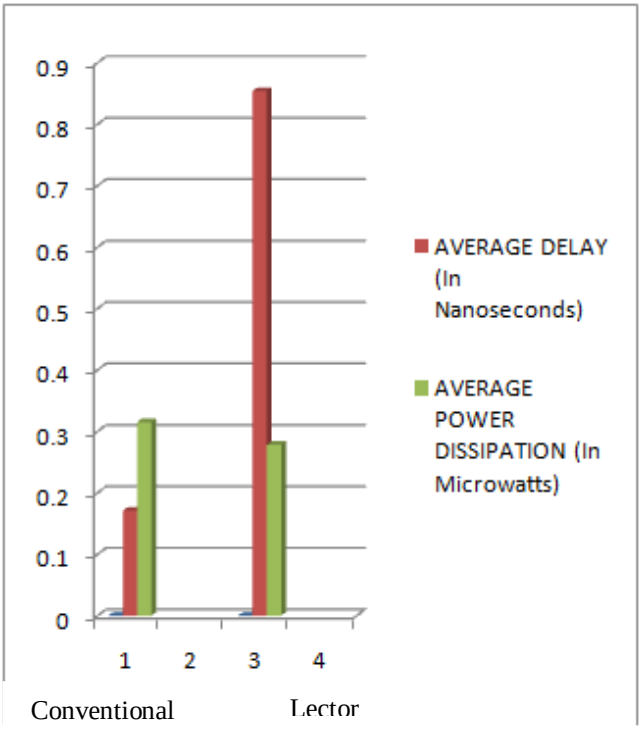

Figure 15 Comparison of Average Delay and average Power for NOR Gate

Implementing the LECTOR technique can reduce power dissipation of the LOGIC CIRCUITS. We can observe the reduction in power dissipation from Conventional to the Proposed LECTOR Technique in Logic Circuits.

The LECTOR technique when applied to generic logic circuits achieves up to 40-45% leakage reduction over the respective conventional circuits without affecting the dynamic power.

It can be concluded from the comparison graphs that the delay is increased in lector technique. Delay can be minimized by increasing aspect ratio. A tradeoff between Propagation delay and area overhead exists here as the delay reduction by sizing the transistors will increase the area overhead. The tool for simulation is TANNER and at 180nm technology and the practical observations has been tabled.

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