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REVIEW ARTICLE

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Design Analysis of AND (2T) and OR (2T) Based Low Power Full Adder Circuit

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Abstract: With the increase in demand for circuits with lower power dissipation, we put forward the following Full Adder circuit. New method is proposed to implement the Full Adder functions. The main design objective for this Full Adder circuit is low power dissipation. The AND and OR gates in the Full Adder circuit (CMOS logic) are replaced by 2T AND and 2T OR gates. The proposed designs are compared with previously known circuits and they show to provide superior performance. The proposed circuit is verified using Tanner EDA v15.0 Tool.

Keywords: AND gates, OR gates, XOR gates, Full Adder

I. INTRODUCTION

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for digital systems. The use of integrated circuits in high performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. This trend is expected to continue, with very important implications for power-efficient VLSI and systems designs. Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. Excessive power dissipation in integrated circuits not only discourages their use in portable environment but also causes overheating which reduces chip life and degrades performance Thus, today there is an increasing need of the portable applications requiring small-area low- power high throughput circuitry. As we know AND and OR gates are important elements in many variant circuit designs, this is especially useful in situations when cost is a factor and for modularity. The two transistor AND and OR gates have only either VDD or GND, thus preventing the flow of short circuit current. Therefore study on these gates is inevitable and any modifications made to these gates would affect the system as a whole. The images of new 2T AND and OR gates are shown.(Figure 1.)

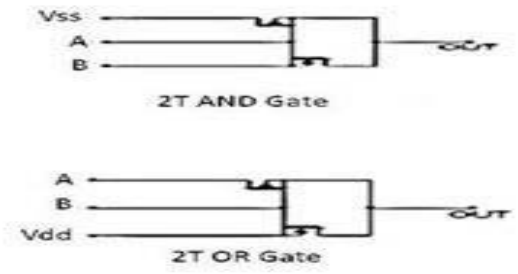

Figure 1. New Gates

II. EXPERIMENTAL DESCRIPTION

The 2T AND gate works as follows
When A and B are logic '0' respectively, NMOS is in OFF state and PMOS is in ON state, therefore the VSS flows to the output which is logic '0'.

When A and B are logic '0' and logic '1' respectively, NMOS is in OFF state and PMOS is in ON state, therefore the VSS flows to the output which is logic '0'.

Similarly A=logic '1' B=logic '0' and A=logic '1' B=logic '1' can be explained The images of simulation of 2T AND gate using Tanner tool v15.0 are shown

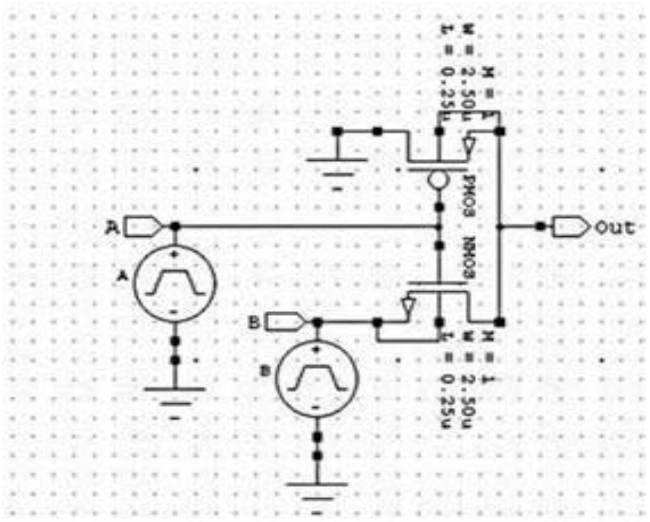

Figure 2. 2T AND Gate

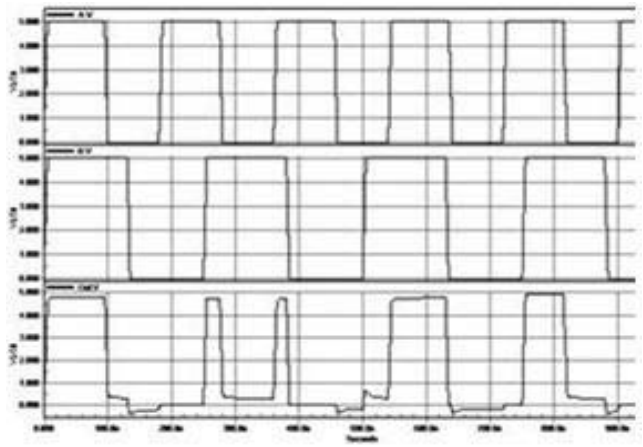

Figure 3. Output of 2T AND Gate

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The 2T OR gate works as follows

When A and B are logic '0' respectively, NMOS is in OFF state and PMOS is in ON state, therefore the A flows to the output which is logic '0'.

When A and B are logic '0' and logic '1' respectively, PMOS is in OFF state and NMOS is in ON state, therefore the Vdd flows to the output which is logic '1'.

Similarly A=logic '1' B=logic '0' and A=logic '1' B=logic '1' can be explained.

The images of simulation of 2T OR gate using Tanner tool v15.0 are shown.

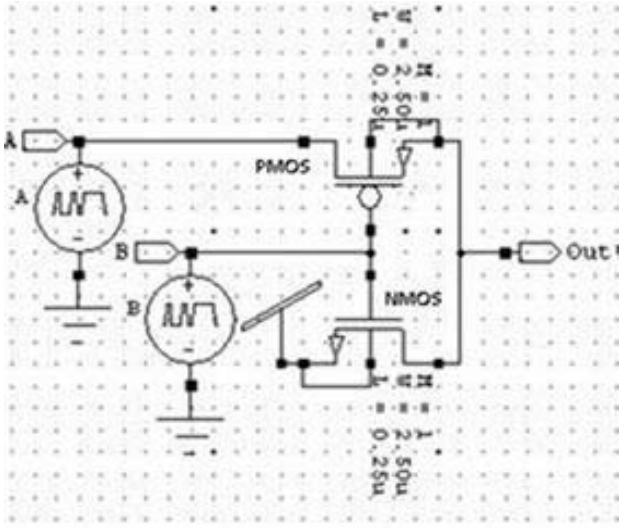

Figure 4. 2T OR Gate

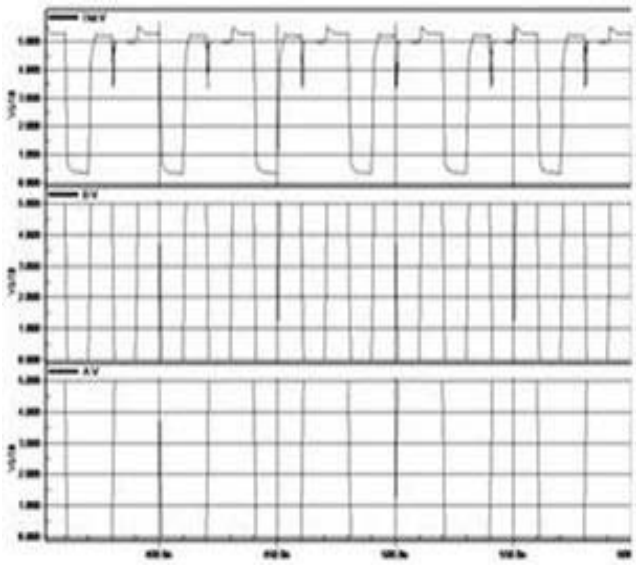

Figure 5. Output of 2T OR Gate

III. PROPOSED FULL ADDER CIRCUITS

In this paper four full adder circuits have been verified, they are

a. CMOS Full adder .
b. CMOS Full adder using new gates.
c. Full adder using only CMOS NAND gates.
d. Full adder using new NAND gates.
e. All the above circuits are verified using Tanner EDA v15.0

a) CMOS Full Adder

The circuit diagram is shown in Figure 5.

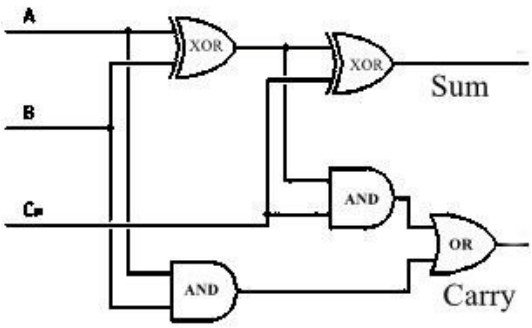

Figure 6. Full Adder

The XOR gate, AND gate and OR gate are implemented using CMOS(shown in Figure 7, Figure 8, Figure 9) and the power is calculated to be 2.3991501mW.

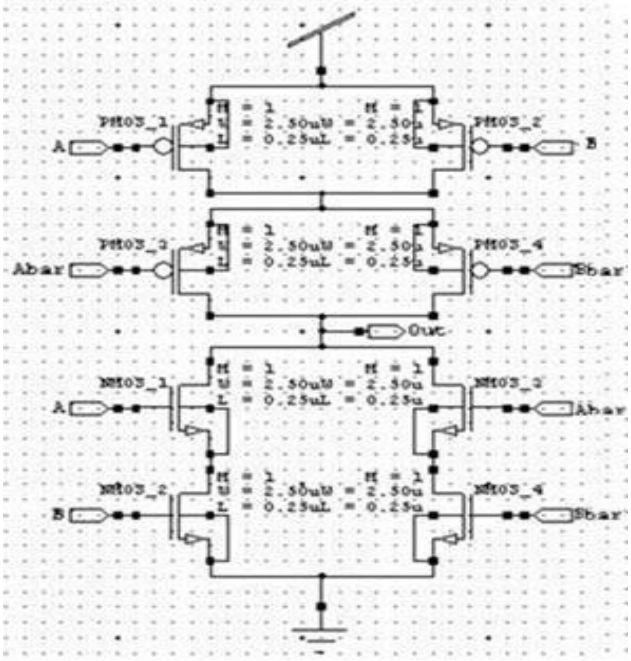

Figure 7.Two input CMOS XOR Gate

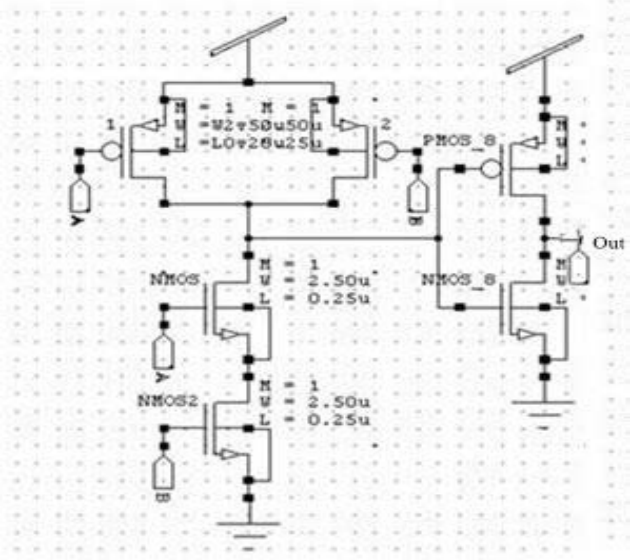

Figure 8. Two input CMOS AND Gate

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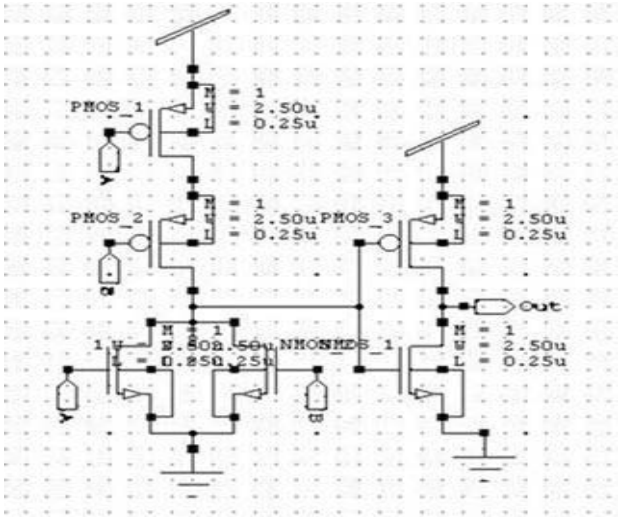

Figure 9. Two input CMOS OR Gate

b) CMOS Full Adder with new gates

Here the AND gates and OR gate of Figure 6. are replaced by new AND and OR gates (Figure 2 and Figure 4) and the power is calculated to be 2.2138266mW.

c) Full Adder using only CMOS NAND gates. The circuit is shown in Figure 10.

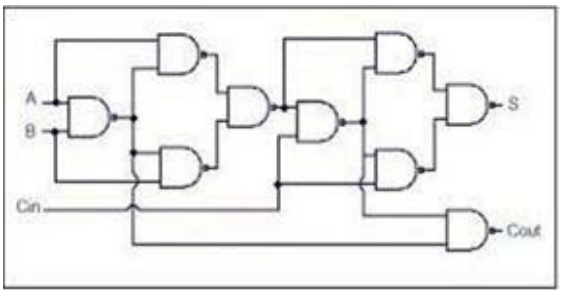

Figure 10. Full Adder using only NAND Gates

The NAND gates shown in Figure 10. are implemented using CMOS as shown in Figure 11.

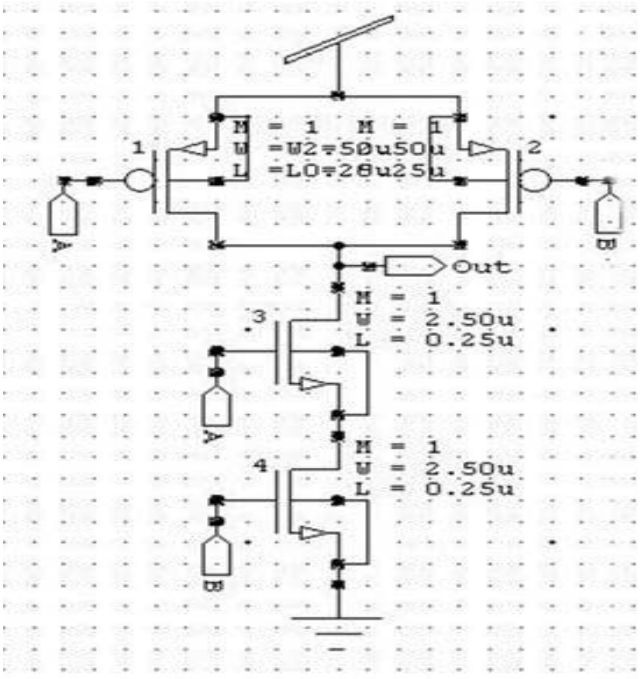

Figure 11. Two input CMOS NAND Gate The power is calculated to be 2.5311997mW.

d) Full Adder using new NAND Gates

The NAND gates shown in Figure 10. are replaced by new NAND gates(as shown in Figure 12) formed using new gates(Figure 1).

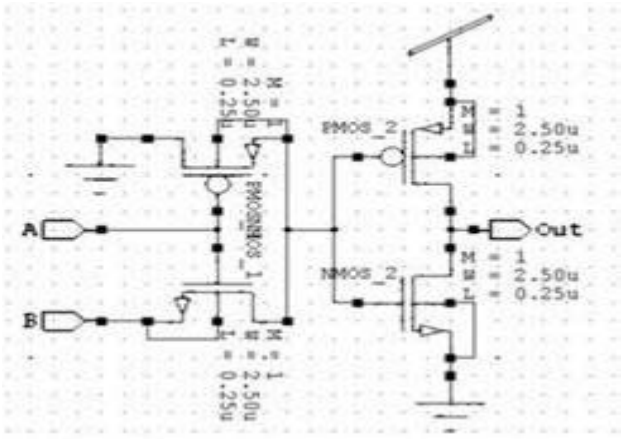

Figure 12. Two input new NAND Gate The power is calculated to be 2.4883064mW.

Table 1. Power comparison table

Circuit	Power (in mW)
CMOS Full adder	2.6847767
CMOS Full adder with new gates	1.5146892
Full adder using only CMOS NAND gates	2.5311997
Full adder using only new NAND gates	2.4883064

IV. CONCLUSIONS

It has been observed that when a Full Adder is implemented using new gates the power has been reduced and also they show superior performance over their counterparts.

V. FUTURE SCOPE

The new gates can be used in other applications which have AND/NAND, OR/NOR circuits in it the use of these gates will result in reduction in power.

VI. REFRENCES

[1]. M.F. Cowlishaw, “Decimal Floating-Point: Algorithm for Computers”, Proc. 16th IEEE Symp. Computer Arithmetic, pp. 104-111, June, 2003.

[2]. Yingtao Jiang et.al,"A Novel Multiplexer-Based Low- Power Full Adder", IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 51, no. 7, july 2004 .

[3]. A.P. Chandrakasan, S. Sheng and R. W. Brodersen," Low-Power CMOS Digital Design", IEEE Joumal of Solid State Circuits Vol. 27, No.:, pp. 473-483.

[4]. N. Weste and K. Eshraghian, “Principles of CMOS VLSI Design, A System Perspective”, MA: Addison- Wesley, 1993 .

[5]. Yu-Ting Pai and Yu-Kumg Chen,"The Fastest Carry Lookahead Adder",Proceedings of the Second IEEE

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Schedule: 28-29 March 2014

International Workshop on Electronic Design, Test and Applications (DELTA'04),434-436.

[6]. H. T. Bui, A. K. Al-Sheraidah, and Y. Wang, "Design and analysis of 10-transistor full adders using novel XOR-XNOR gates," in Proc. Int. Conf. Signal Processing 2000 (Wold Computer Congress), Beijing, China, Aug. 2000.

[7]. J.Wang, S. Fang, andW. Feng, "Newefficient designs for XOR and XNOR functions on the transistor level," IEEE J. Solid-State Circuits, vol. 29, pp. 780-786, July 1994.

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