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Reduced Hardware Cordic Based 16 Point Fft Processor

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Abstract: This project presents a 16 point FFT processor based on a Reduced Hardware CORDIC Algorithm. The proposed algorithm utilizes a new rotation scheme which uses only two angles as the rotation angles. In this proposed scheme, we do not want to store the twiddle angles. Thus there is reduction in the number of hardwares required, which results in a considerable reduction in the power and total memory used. Then the performance of 16 point FFT processor based on proposed reduced hardware CORDIC algorithm is compared with 16 point FFT processor based on conventional CORDIC algorithm. The synthesis results match the theoretical analysis and it can be observed that more than 50% reduction can be achieved in total memory used. In addition, the dynamic power consumption can be reduced by as much as 30% by reducing memory accesses.

Keywords: Cooley- Tukey, CORDIC, FFT, low power, VLSI

I. INTRODUCTION

For a long time, the field of Digital Signal Processing has been dominated by Microprocessors. This is mainly because they provide designers with the advantages of single cycle multiply-accumulate instruction as well as special addressing modes. Although these processors are cheap and flexible they are relatively slow when it comes to performing certain demanding signal processing tasks like Discrete Fourier Transform, Image Compression, Digital Communication and Video Processing. Of late, rapid advancements have been made in the field of VLSI and IC design. It is the duty of VLSI design engineers to make the VLSI implementation of digital signal processing operations possible. VLSI implementation of Digital Signal Processing is what we termed as VLSI Signal Processing. VLSI implementation of DSP operations directly requires large number of hardware components such as multipliers, ROMs.

Discrete Fourier Transform (DFT) is one of the core operations in Digital Signal Processing and communication systems. Many fundamental algorithms can be realized by DFT, such as convolution, spectrum estimation, and correlation. Furthermore, DFT is widely used in standard embedded system applications such as wireless communication protocols requiring Orthogonal Frequency Division Multiplexing [1] and Radar Image Processing using Synthetic Aperture Radar and Software Defined Radio. However, DFT is difficult to implement directly due to its computational complexity. In practice, Fast Fourier transform (FFT) is used for reducing the complexity of computations. A typical FFT processor is composed of butterfly calculation units, memory banks and control logic (address generator for data and twiddle factor accesses). For FFT processors, butterfly operation is the most computationally demanding stage. Traditionally, a butterfly unit is composed of complex adders and multipliers.

The Coordinate Rotation Digital Computer (CORDIC) algorithm is an alternative method to realize the butterfly operation [3,4] without using any dedicated multiplier hardware. CORDIC algorithm is versatile and hardware efficient since it requires only add and shift operations, making it suitable for the butterfly operations in FFT. Instead of storing actual twiddle factors in a ROM, the CORDIC-based FFT processor needs to store only the twiddle factor angles in a ROM for the butterfly operation. Additionally, the CORDIC-based butterfly can be twice faster than traditional multiplier-based butterflies in VLSI implementations. Even though not using any multipliers in CORDIC Algorithm, there is an increase in the number of hardware such as shifters. In this paper, we are modifying the CORDIC algorithm there by reducing the number of hardware and thus power. With this reduced hardware CORDIC, a 16 point FFT processor is implemented.

The organization of the paper is as follows: In Section 2, CORDIC algorithm fundamentals and the design of CORDIC-based FFT processor are described. The proposed reduced hardware CORDIC algorithm and it's hardware

architecture are presented in Section 3 for radix-2 16 point FFT. Hardware synthesis results are discussed in Section 4.

II. FFT AND CORDIC ALGORITHM

The N-point discrete Fourier transform is defined by

$X(K) = \sum_{n=0}^{N-1} x(n) w_N^{kn}$ (1)

Where $w_N = e^{-j2\pi/N}$, is the so-called "twiddle factor". For N-point FFT, there are $\log_2$N stages and each stage contains N/2 butterfly operations. The following equations describe the radix-2 butterfly operation at stage m.

$X_{m+1}(p) = X_m(p) + X_m(q)$ (2)

$X_{m+1}(q) = (X_m(p) - X_m(q)) * W_N^{Kn}$ (3)

CORDIC algorithm was proposed by J.E. Volder [2]. It is an iterative algorithm to calculate the rotation of a vector by using only additions and shifts. Figure 1 shows an example for rotation of a vector Vi.It can be shown that rotation can be simplified to:

$x_{i+1} = x_i - x_i . d_i . 2^{-i}$ (4)

$x_{i+1} = x_i - x_i . d_i . 2^{-i}$ (5)

Here, the direction of each rotation is defined by d_i and the sequence of all d_i 's determines the final vector. d_i is given as

$d_i = {+1 \; if \; z_i \geq 0 \atop -1 \; if \; z_i < 0}$ (6)

where zi is called angle accumulator and given by

$z_{i+1} = z_i - d_i . \arctan \; 2^{-i}$ (7)

All operations described through Eqs. 4–7 can be realized by only additions and shifts; therefore, CORDIC algorithm does not require dedicated multipliers. CORDIC algorithm is often realized by pipeline structures, leading to high processing speed. Figure 2 shows the basic structure of the pipelined CORDIC unit.

As shown in Eq. 1, the key operation of FFT is x(n). W_N^{Kn} $(w_N = e^{-j2\pi/N})$. This is equivalent to "Rotate x(n) by angle $2\pi kn/N$" operation which can be realized easily by the CORDIC algorithm. Without any complex multiplications, CORDIC-based butterfly can be fast. An FFT processor needs to store the twiddle factors in memory. CORDIC-based FFT doesn't have twiddle factors but needs a memory bank to store the rotation angles. For radix-2, N-point, m-bit FFT, mN/2 bits memory needed to store N/2 angles [5]. In the next section, a new CORDIC FFT design is presented where CORDIC uses only two angles for rotation.

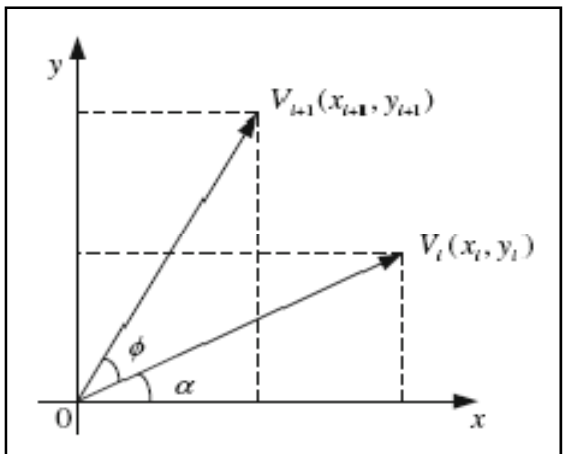

Figure 1. Rotate Vector $v_i(x_i, y_i)$ to $v_{i+1}(x_{i+1}, y_{i+1})$

III. PROPOSED CORDIC BASED FFT

In FFT we need to find cosine and sine of angles which lies in the range 0^0 to 180^0. The conventional CORDIC algorithms are used to handle rotations only in the range of angles [-99°,99°]. Moreover, they are serial in nature and require a ROM to store the lookup table and hardware-expensive barrel shifters. So we go for a reduced hardware CORDIC. Our objective is to reduce the number of barrel shifters compared to conventional CORDIC. This, along with the use of small size multiplexers, is expected to result in considerable savings in FPGA resources (in comparison to conventional CORDIC). This is designed for rotation mode. The key idea in this is representing all the angles in

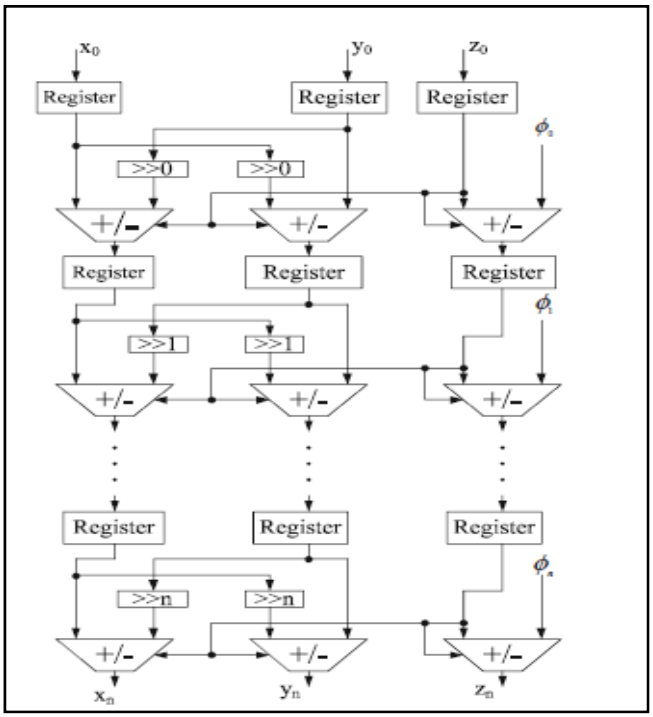

Figure 2. Pipelined CORDIC unit

The range of [0^o,180°] using combinations of two signed elementary angles, $\tan^{-1}$ (1) that is 45^o and $\tan^{-1}$ (2^{-3}) that is 7.12^o . In other words, angle Z ε [0^o,180°] is represented by k0 and k1, where k0 and k1 are two integers which depend on the value of Z. Instead of storing rotation angles we only need to store values of k0 and k1. The angle $\tan^{-1}$ (1) is rotated k0 times and the angle $\tan^{-1}$ (2^{-3}) is rotated k1 times to achieve te desired angle. The elementary angles are chosen as $\tan^{-1}$ (1) and $\tan^{-1}$ (2^{-3}) because corresponding rotations provide architecture for 16 point FFT butterfly with merely shifters and adder and subtractors.

The architecture for proposed CORDIC is shown in Figure 3. The state machine runs k0 + k1 times. It has two outputs: m and stop-bit. One-bit output m is set to 0 for first k0 times and set to 1 for next k1 times. The angle for rotation is $\tan^{-1}(1)$, when m is 0 while it is $\tan^{-1}(2^{-3})$, when m is 1. X and Y are selected by multiplexers M1 and M0 respectively, when m is 0 and shifted values of X and Y (X/8 and Y/8) are selected when m is 1. In this proposed architecture, direction of rotation is always in anticlockwise direction, therefore multiplexer for selecting the direction of rotation can be eliminated. The stop-bit indicates the availability of valid outputs at X and Y output lines and is set to 1 at the end of k0 + k1 cycles. The scaler performs a

correction if the rotation is by $\tan^{-1}(1)$. The required correction of S = 0.707 is implemented by a shifted-adder and subtractor.

The multiplexer requirement is brought down to a few 2 to 1 multiplexers as compared to 2, 8 to 1 multiplexers for same accuracy in conventional CORDIC. In conventional CORDIC, 2 pairs of adder/subtractor is used where as in proposed architecture one adder and subtractor is used. The quantities in ROM are stored in sign-magnitude format to save two's complement logic. For FFT, the values stored in ROM are the rotation values corresponding to angles 0, 22.5°, 45°, 67.5°, 90°, 112.5°,135°, 157.5°, 180° . The following table shows rotation values corresponding to the above given angles for FFT.

Table 1. Value for k_0 and k_1 for angles used in FFT

Angles	*Value for K0*	*Value for K1*
0	0	0
22.5	0	3
45	1	0
67.5	1	3
90	2	0
112.5	2	3
135	3	0
157.5	3	3

Figure 4 shows the architecture for a reduced hardware CORDIC based FFT Butterfly. In conventional CORDIC we are supposed to give the input angles. But in this proposed architecture we only need to give the address of memory location where the values of k0 and k1 are stored. For example suppose our angle is 45°, the twiddle factor is given by $W_{16}^{2} = e^{-\left(\frac{2\pi}{16}\right)*2}$ so our input to CORDIC is 2 instead of angle 45°. In conventional CORDIC, for angles greater than 90, set of iterations have to be repeated 2 times, but in this proposed CORDIC , we are able to rotate up to 180 with single set of iteration.

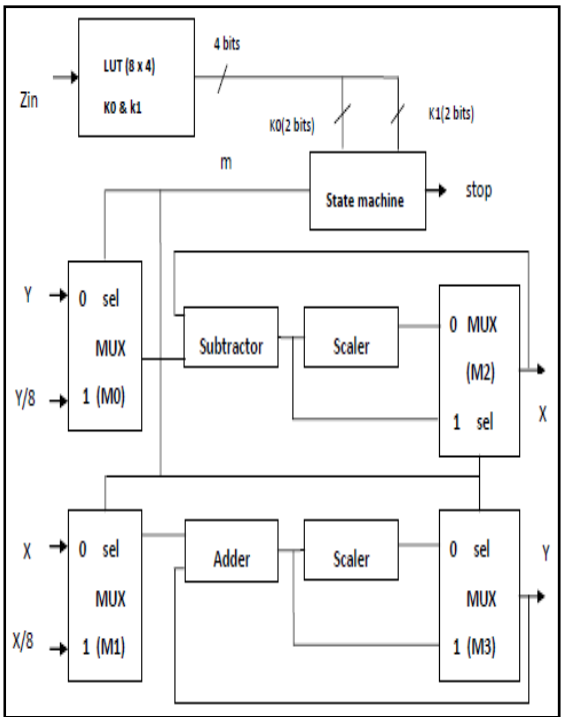

Figure 3. Proposed Reduced Hardware CORDIC

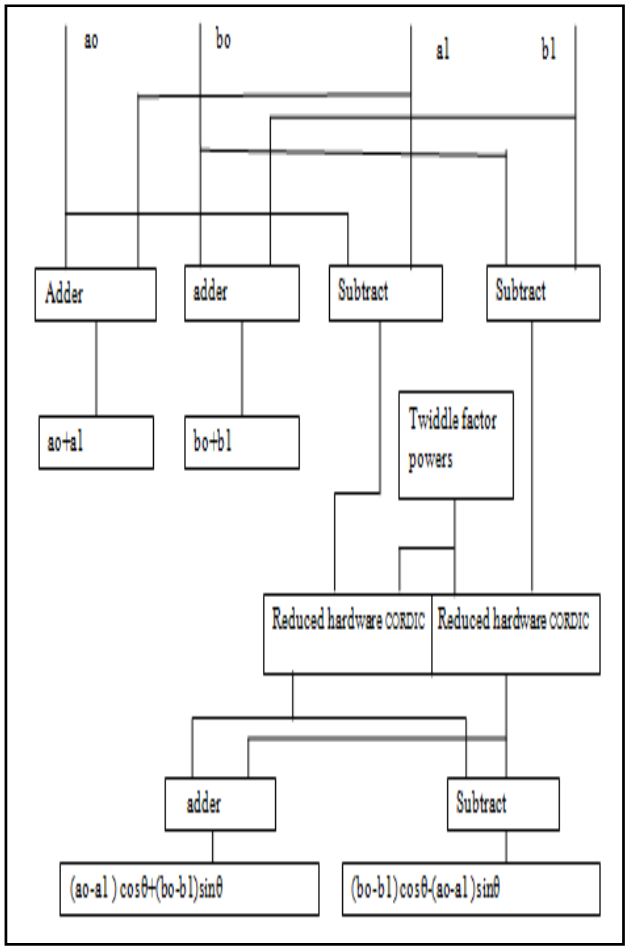

Figure 4. FFT Butterfly using Reduced Hardware CORDIC

IV. EXPERIMENTAL RESULTS

The proposed designs for radix-2 FFT algorithms have been realized by Verilog-HDL and simulated and synthesis using Xilinx ISE 14.1. Synthesis results shown in Table 2 confirm that the proposed design can reduce the total memory used and dynamic power for FFT processors without any tangible increase in the number of logic elements used when compared against the conventional CORDIC implementation (i.e., angles are stored in memory). It was shown that more than 50% of the total memory used is reduced. Furthermore, dynamic power consumption is reduced (up to 30%) with no delay penalties.

Table 2. FFT processor based on Reduced Hardware CORDIC with FFT processor based on Conventional CORDIC

Compared Features	*FFT Processor based on*		
	Proposed Reduced Hardware CORDIC	*Conventional CORDIC*	
Dynamic Power	0.412W	0.642W	
Total onchip power	1.143W	1.379W	
Delay	5.512ns	48.831ns	
Maximum Frequency	181.427MHz	20.479MHz	
Total Memory used	444996Kb	1203024Kb	

V. CONCLUSION AND FUTURESCOPE

CORDIC is a powerful algorithm, and a popular algorithm of choice when it comes to various Digital Signal Processing applications. Implementation of a CORDIC-based processor on FPGA gives us a powerful mechanism of implementing complex computations on a platform that

provides a lot of resources and flexibility at a relatively lesser cost. Further, since the algorithm is simple and efficient, the design and VLSI implementation of CORDIC based processor is easily achievable. CORDC is further modified to reduce memory used and dynamic power and using that FFT is implemented. FFT designed using modified CORDIC is compared with FFT designed using conventional CORDIC. . It is seen that total memory used and power of FFT processor based on Reduced Hardware CORDIC is less compared to FFT processor based on conventional CORDIC. Operation frequency of modified architecture is also increased.

Although this project primarily deals with the design of 16-point FFT using modified CORDIC algorithm, the concept and the architecture can be extended to calculate the higher order FFTs, thus, providing a fast, low-cost implementation of processors for Image Processing and other Digital Signal Processing Applications. The performance of this FFT processor based on modified CORDIC algorithm can also be compared with that of a FFT processor designed using distributed arithmetic. Reduced Hardware CORDIC can also be used for implementing other Digital Signal Processing Operations and Image Processing Operations such as DCT.

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